Technology-Independent CMOS Op Amp in Minimum Channel Length

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Technology-Independent CMOS Op Amp in Minimum Channel Length

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To my wife, Proma, my son, Sidharth, and my parents

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SUMMARY

The performance of analog integrated circuits is dependent on the technology. Digital circuits are scalable in nature, and the same circuit can be scaled from one technology to another with improved performance. But, in analog integrated circuits, the circuit components must be re-designed to maintain the desired performance across different technologies. Moreover, in the case of digital circuits, minimum feature-size (short channel length) devices can be used for better performance, but analog circuits are still being designed using channel lengths larger than the minimum feature sizes.

The research in this thesis is aimed at understanding the impact of technology scaling and short channel length devices on the performance of analog integrated circuits. The operational amplifier (op amp) is chosen as an example circuit for investigation. The performance of the conventional op amps are studied across different technologies for short channel lengths, and techniques to develop technology-independent op amp architectures have been proposed. In this research, three op amp architectures have been developed whose performance is relatively independent of the technology and the channel length. They are made scalable, and the same op amp circuits are scaled from a 0.25 μm CMOS onto a 0.18 μm CMOS technology with the same components. They are designed to achieve large small-signal gain, constant unity gain-bandwidth frequency and constant phase margin. They are also designed with short channel length

transistors. Current feedback, g_m boosted, CMOS source followers are also developed, and they are used in the buffered versions of these op amps.

Chapter 1

Introduction

Most analog integrated circuits are fabricated in digital CMOS technologies. In the past years, the performance of digital CMOS circuits has improved with advances in the digital technology. The minimum feature size has been constantly getting scaled down, which has imparted the capability to build digital circuits with smaller area, high speed, and reduced parasitics. But, analog circuits are still being made using longer channel length transistors due to the degrading effects of smaller channel length on the circuit performance. Digital circuits are scalable in nature, i.e., with course of time; the same circuit has been scaled onto an improved technology with little re-work. But, in case of analog circuits, when moving from an older to a newer technology, the aspect ratios of most of the transistors need to be redesigned to maintain the desired performance. The research in this thesis is aimed at developing analog circuit design techniques for

- Scalable architectures with technology-independent performance
- Use of all minimum feature-size channel length transistors in the design

An operational amplifier (op amp) was chosen as the example circuit. Three op amp architectures, namely *OP*1, *OP*2, and *OP*3 were developed to verify technology-independent performance. A g_m boosted source follower was also developed, and it was integrated with the op amps to buffer their outputs.

The first op amp architecture, *OP*1, was designed to achieve constant small-signal gain and phase margin when scaled as-it-is onto different technologies. It was designed using all minimum feature-size channel length devices in the corresponding technologies. This architecture was simulated using the BSIM3v3 models in a 0.25 μm CMOS process and a 0.18 μm CMOS process with minimum feature-size channel lengths in each of them. This architecture was not fabricated and only the simulation results are presented.

The second op amp architecture, *OP*2, was designed to achieve maximum small-signal gain and constant phase margin when scaled as-it-is onto different technologies. It was also designed using all minimum feature-size channel length devices in the corresponding technologies. This op amp was fabricated in both the 0.25 μm CMOS and the 0.18 μm CMOS processes. The simulated and measured results for this architecture are presented. In this op amp, a technology-independent bias circuit, which uses an adaptive PMOS bulk drive mechanism to bias the transistors of the op amp, was also fabricated, and the results are presented.

The third op amp architecture, *OP*3, was designed to achieve maximum small-signal gain, constant unity gain-bandwidth frequency, and constant phase margin when scaled as-it-is onto different technologies. It was designed using channel lengths, which were twice as large as the minimum feature-size in the corresponding technologies. The simulated and measured results for this architecture in both the CMOS processes are presented.

Three circuit topologies of g_m boosted source followers using current feedback were developed, and one of them was used to buffer the outputs of the op amps. The performance of these source followers was dependent on the technology parameters. The buffered op amps were fabricated in both the 0.25 μm CMOS and the 0.18 μm CMOS processes. The simulated and measured results for this architecture are presented.

The organization of the thesis is as follows. In Chapter 2, various implications of using small channel length devices on the circuit performance are studied. The technology also has a major influence on the circuit performance, and its effect on two commonly used op amp configurations are studied in this chapter. Two gain stages: one with constant gain and the other with maximum gain are developed while using all small channel length devices. Finally, this chapter concludes with the development of an approximate technique to bias a MOS device at the onset of weak inversion.

In Chapter 3, the transistor-level implementation of the gain stages, developed in Chapter 2, are presented along with their biasing scheme. A negative resistance scheme is used to boost the small-signal gain of these gain stages. The effect of various non-idealities (like, bulk-effects) in these gain stages are also discussed in this chapter.

In Chapter 4, two versions of the two-stage Miller compensated op amp is developed using the gain stages from the previous chapters. The architecture of this op amp is made scalable for easy migration across different technologies. These op amps are designed to achieve appreciable small-signal gain and constant

phase margin across different technologies. Various performance specifications of the op amps are investigated for small channel length and technology-independent performance. This chapter concludes with the simulation and measurement results for these op amps.

In Chapter 5, a technology-independent op amp with large small-signal gain and constant unity gain-bandwidth frequency and phase margin is developed. A constant g_m biasing scheme along with the compensation of the op amp is discussed in this chapter. The chapter concludes with the simulation and measurement results for this op amp.

In Chapter 6, buffered versions of the op amps, developed in the previous chapters, are presented. The op amps are buffered using g_m boosted source followers using current feedback. The simulation and the measurement results for the source followers and the buffered op amps are presented in this chapter.

Lastly, in Chapter 7, contributions of this research and the scope of future work are discussed.

Chapter 2

Implications of Short Channel Length and Technology Dependence on Circuit Performance

Analog integrated circuits are primarily fabricated in standard digital CMOS processes. The improvements in digital CMOS technologies have made way for improvements in the analog circuits. The advances in digital CMOS processes have allowed the shrinking of device dimensions to 90 nm or smaller. The performance of digital circuits has improved largely due to shrinking of the device sizes. Though the digital process can support extremely small channel lengths, analog circuits are still designed using long channel transistors in order to achieve the desired circuit performance. As in the case of the digital circuits, scaling down of the device geometries in the analog circuits could improve circuit performance in terms of lower area, reduced parasitics, higher speed, low-voltage low-power operation among others. But, the use of all small channel length devices has always been avoided while designing analog circuits. Sometimes, in order to partially achieve the advantages of small channel lengths, a mixed design, which uses a mixture of both small channel length devices as well as large channel length devices, has been used to build analog circuits. Some of the major degrading factors arising as a result of the use of small channel length devices are as follows:

i. Small channel length transistors have large channel length modulation effects that reduce the small-signal drain-to-source resistance drastically.

ii. Decreasing the channel length causes a decrease in the effective channel area below the gate of the MOS transistor. Mismatch and noise are inversely proportional to the effective area, and they become large with smaller channel lengths.

iii. Smaller channel length transistors are also very difficult to dc bias, and they tend to introduce non-idealities in the conventional dc biasing schemes such as current mirroring. In a current mirror, when the devices are operated in strong inversion, large channel length modulation effects cause a wide variation in the drain current as a function of the output voltage. This becomes even worse in weak inversion due to the exponential dependence of the drain current on the drain voltage.

Conventional analog circuit architectures cannot overcome most of these problems. New architectures and design techniques are needed to make analog circuits work properly with minimum channel lengths. References to research work involved in circuit design with minimum channel lengths are limited [2]-[16]. Based on the past modeling, simulation and experimental work done in the area of sub-micron CMOS design, the effects of smaller channel lengths on circuit performance, like, dc biasing, small-signal gain, mismatch, supply voltage limits, noise, high frequency performance, and distortion are briefly studied in the following sections.

2.1 DC Biasing

Proper dc biasing of an analog circuit is the first step towards achieving the desired performance. Most of the analog circuits are current biased using various current sources and sinks [1]. It is important to study the effect of smaller channel lengths on the performance of these current sources and sinks.

In a current sink (or a source), it is desired that the output current remains fairly constant over a wide output voltage range, i.e., the output resistance should be large, and the magnitude of current should remain fairly constant. The lower limit of the output voltage range, where the current tends to vary, can be referred to as $V_{\min}$. This minimum output voltage, $V_{\min}$, can be visualized as a point at which the current sink starts to deviate largely from its ideal behavior (this happens when the mirrored transistor moves from saturation into the triode region of operation). When using small channel length devices, the current mirroring does not remain constant over the output voltage range primarily due to large channel length modulation effects.

Four different types of NMOS current sinks are considered in this section, and their performance with different channel lengths ($1.3\,\mu m$, $0.4\,\mu m$ and $0.25\,\mu m$) is studied through simulations.

a) Simple NMOS Current Sink

The simple NMOS current sink, shown in Figure 2.1, is the most commonly used current mirror used for biasing. This circuits works well for longer channel lengths, but its performance degrades largely with decreasing channel lengths. As the channel length becomes smaller, the drain current suffers from large channel length modulation effects in the saturation region (as seen in Figure 2.1). Thus, for smaller channel lengths, this scheme is not suitable for biasing.

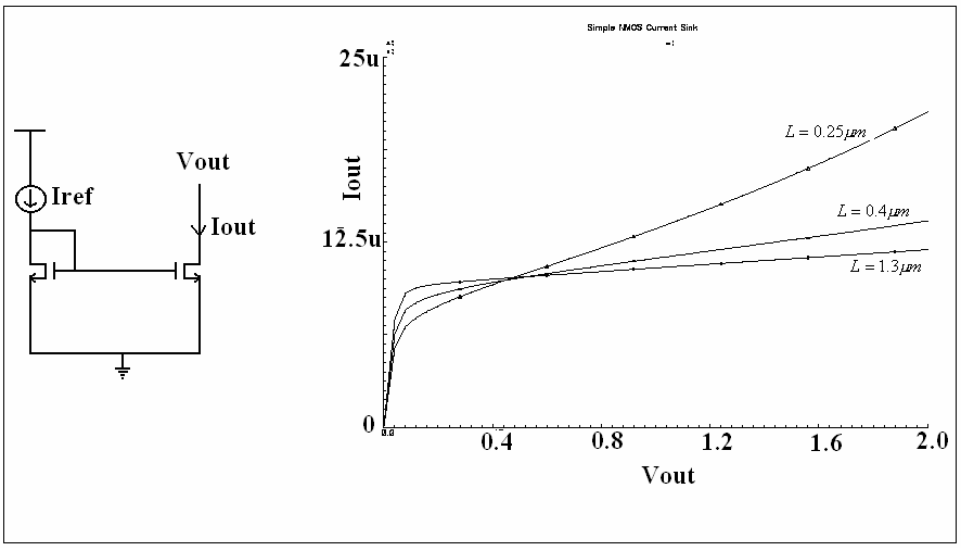


Figure 2.1. Simple NMOS current sink

b) Cascode NMOS Current Sink

In the cascode NMOS current sink, shown in Figure 2.2, due to the cascoded output stage (which gives high output resistance), the drain current remains fairly

constant for smaller channel lengths over the output voltage range. But in this scheme, the value of the minimum output voltage, $V_{\min}$, for proper mirroring operation is large, and it is not suitable for use in circuits operated with smaller power supplies. The voltage supplies for the present day analog circuits are being scaled down for low power applications, and most of the current CMOS technologies cannot tolerate more than 3 V. Thus, it is very important that the value of $V_{\min}$ be kept fairly small.

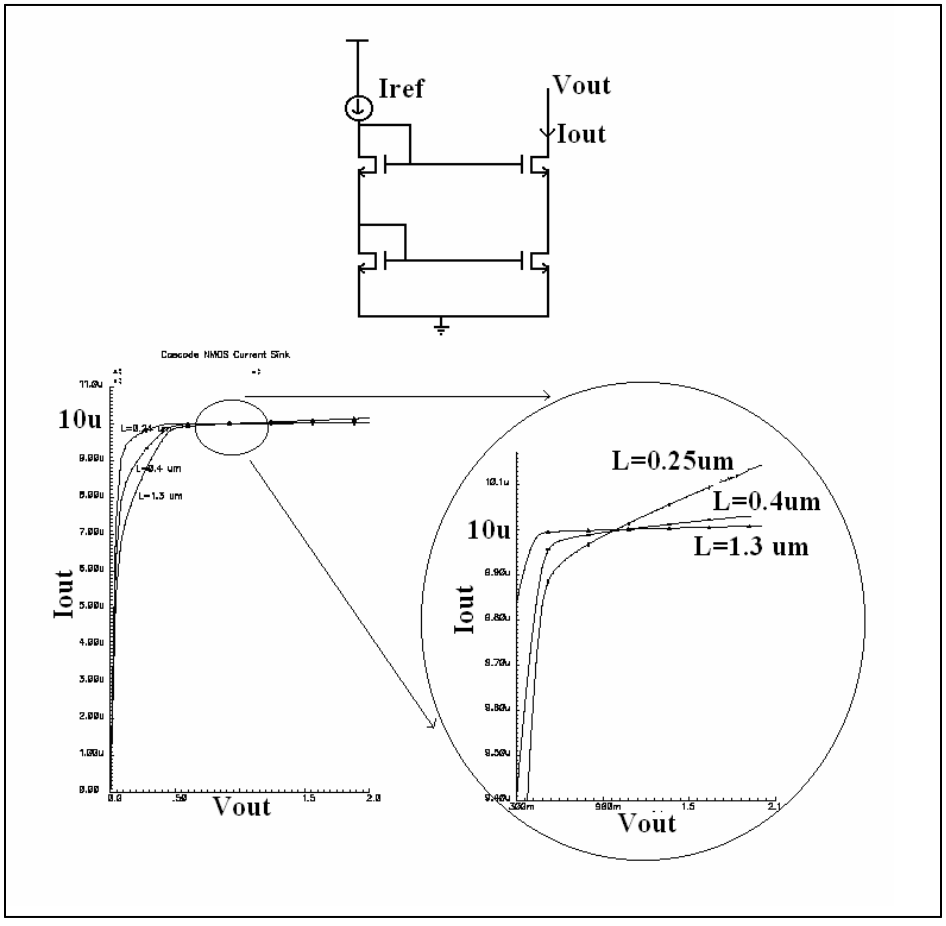


Figure 2.2. Cascode NMOS current sink

c) Self-biased Cascode NMOS Current Sink

The self-biased NMOS cascode current sink, shown in Figure 2.3, shows better performance over the cascode current sink for smaller channel lengths. It has a smaller value of $V_{\min}$, and it also shows relatively constant current over the output voltage range. This architecture can be used as a relatively simple biasing scheme for small channel length devices. However, this circuit has problems when the bias current is small. It requires a large value of the resistor to generate smaller biasing currents, which becomes a limitation in terms of the area and accuracy of the integrated resistor.

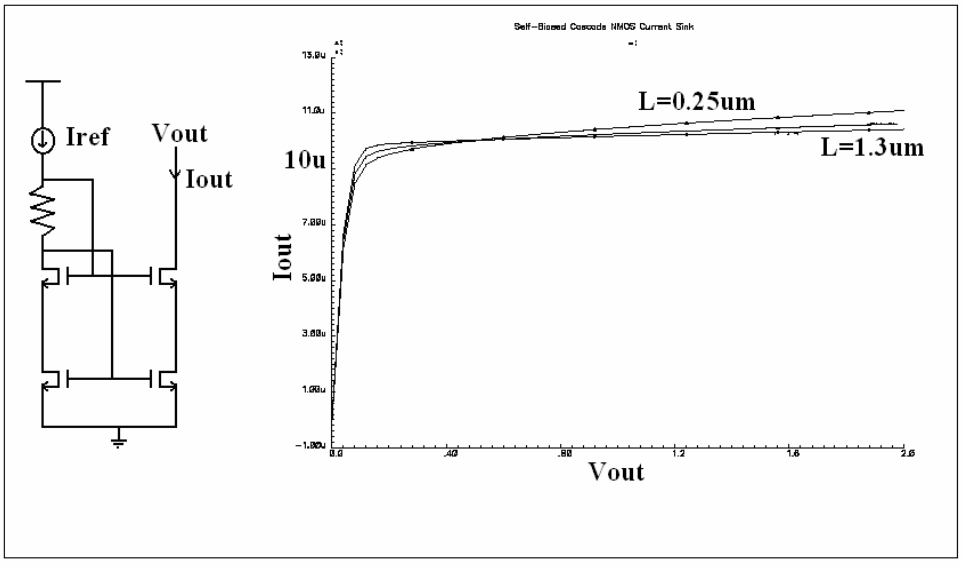


Figure 2.3. Self-biased cascode NMOS current sink

d) High-swing Cascoded NMOS Current Sink

The high-swing cascoded NMOS current sink is shown in Figure 2.4. It can be seen that even with smaller channel lengths, the mirrored current remains appreciably constant over a wide output voltage range, and the value of $V_{\min}$ is also small. This biasing scheme seems to be the best while using small channel length devices, but an extra biasing voltage needs to be generated to bias the upper NMOS transistors.

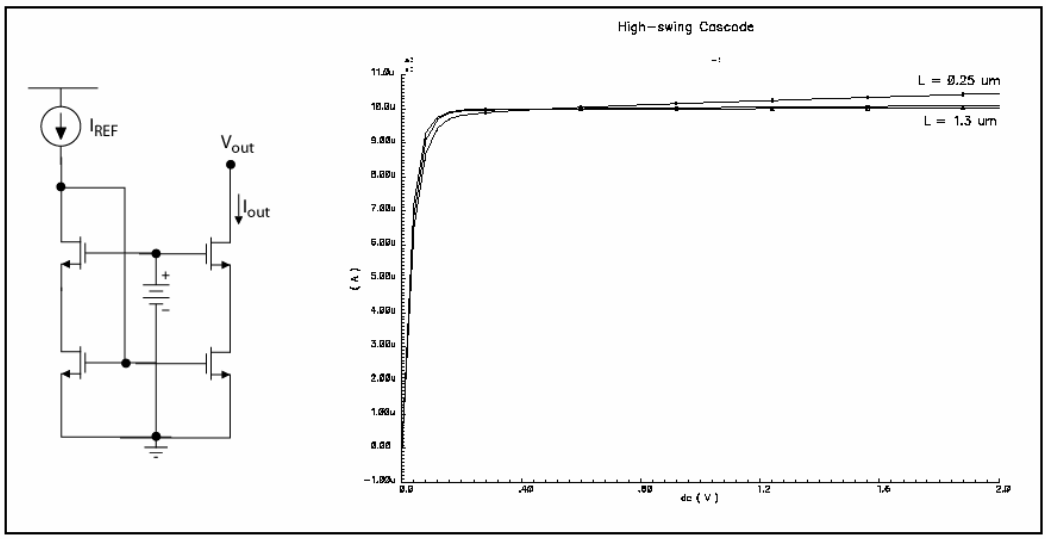


Figure 2.4. High-swing cascoded NMOS current sink

2.2 Small-Signal Gain

In most of the analog circuits, small-signal ac voltage gain is one of the most important performance specifications. For a long channel, square law MOS device, the transconductance (g_m) in moderate and strong inversion is given by

$$g_m = \sqrt{2K' \frac{W}{L} I} \tag{2.1}$$

where, $K' = \mu C_{ox} = \mu \frac{\varepsilon_{ox}}{t_{ox}}$

ε_{ox} is the gate oxide permitivity, and t_{ox} is the oxide thickness. The above expression of transconductance assumes a square-law model, but for smaller channel lengths, the drain current model tends to become linear, primarily due to the degradation of mobility with decreasing channel length. While using small channel lengths, the expression for the drain current and the transconductance becomes mathematically intensive and complicated. Thus, Equation (2.1) is a simple approximation (generally an under estimation) of the transconductance for small channel lengths. With improvements in CMOS technology, the channel lengths of the devices have shrunk down, which gives large transconductance. The oxide thickness has also decreased causing an increase in the transconductance of the device. On the other hand, smaller channel lengths cause large channel length modulation effects. The drain-to-source resistance, r_{ds} , of the device is given by

$$r_{ds} = \frac{V_A}{I} \tag{2.2}$$

where, the Early voltage, V_A, decreases strongly with smaller channel lengths causing a decrease in r_{ds} (shown in Figure 2.5). As an example, the Early voltage for a channel length of 0.5 μm in a 0.18 μm CMOS process was found to be 3.6 V. Overall, the small-signal gain, given by the product of g_m and r_{ds}, is significantly reduced due to smaller channel lengths. The variation in small-signal voltage gain with varied channel lengths was studied through simulations and is shown in Figure 2.6. In these simulations, the channel lengths were varied, but the aspect ratio was kept the same in each case.

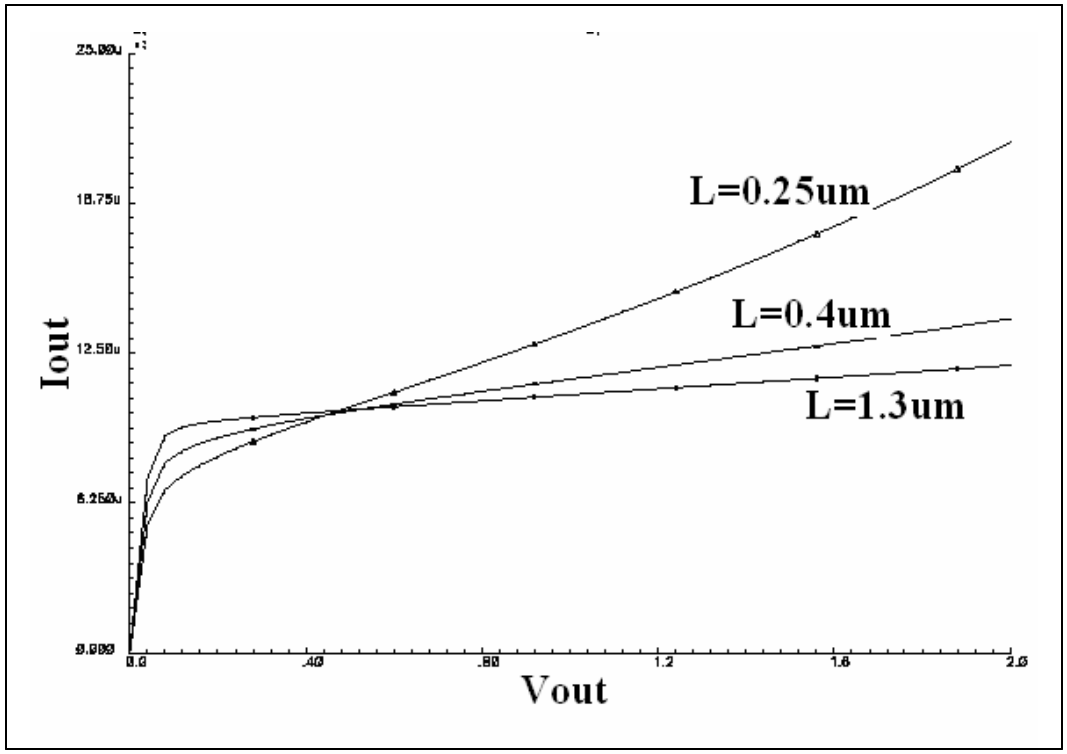
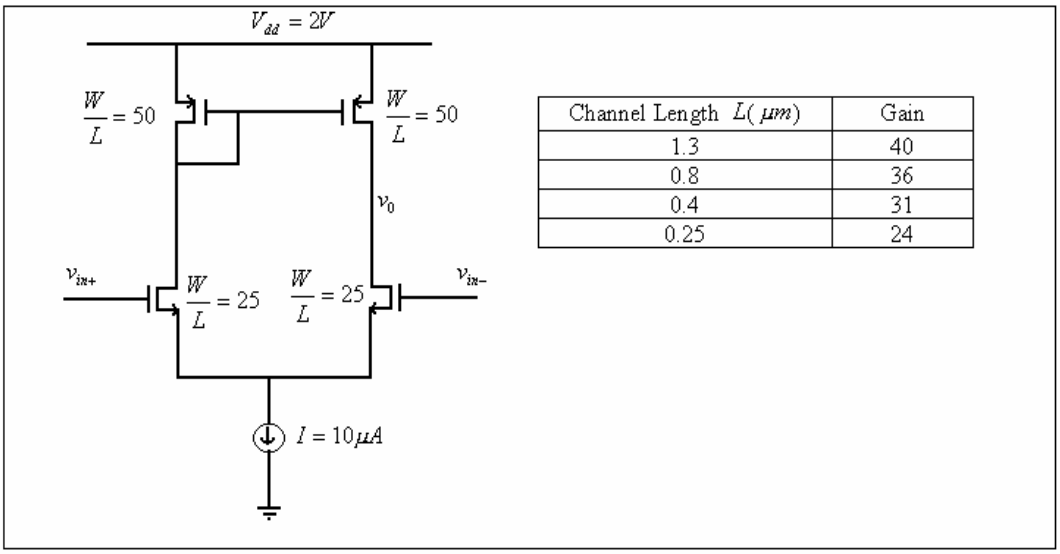


Figure 2.5. Channel length modulation effect with varied channel lengths



Channel Length $L(\mu m)$	Gain
1.3	40
0.8	36
0.4	31
0.25	24

Figure 2.6. Variation in small-signal gain for different channel lengths

2.3 Mismatch

Mismatch in MOS transistors is a very serious issue, especially in high-precision analog circuits (like an operational amplifier). Mismatch in CMOS circuits gives rise to voltage and current offsets that degrade the circuit performance. Mismatch can be broadly classified into two types: Mismatch due to processing, and mismatch in design. Mismatch due to processing occurs in the fabrication phase, where devices with identical geometries in design have mismatched geometries after fabrication due to processing defects and limitations. Mismatch in design is caused in the design phase due to mismatched biasing conditions in the circuit. This kind of mismatch gives rise to an offset referred to as "systematic offset". Examples of mismatch in design could be as follows:

i. In a differential input pair consisting of two identical MOS transistors with equal input voltages, they carry different currents.

ii. In a current mirror circuit, the mirrored and the reference currents are mismatched.

In most cases, the mismatches in the design phase are eliminated using various design techniques. Most of the final offsets present in the circuit are caused during processing resulting in mismatches in transistor geometries. A lot of work has been done in characterizing MOS transistor mismatches through analytical modeling and experimental results [2-10]. The understanding of mismatch in MOS transistors is largely based on analytical equations whose parameters have been extracted from experimental results. Physics-based equations explaining mismatch has not been fully explored. All of these mismatch analyses (except [7] and [9]) do not consider devices with extremely small channel lengths (like, $0.35\mu m$, $0.25\mu m$, $0.18\mu m$ or less). In [7] and [9], mismatch analysis on transistors with channel lengths as low as $0.24\mu m$ has been studied through experimental data.

The saturated drain-current equation, in a simplified form, can be given by

$$I_D = \beta \frac{(V_{GS} - V_T)^2}{2}(1 + \lambda V_{DS}) \tag{2.3}$$

where, $\beta = \mu C_{OX} \frac{W}{L}$, V_T is the threshold voltage, and λ is the channel length modulation parameter. The threshold voltage can be expressed as [2]

$$V_T = \phi_{MS} + 2|\phi_F| + \frac{Q_D}{C_{OX}} - \frac{Q_{SS}}{C_{OX}} \tag{2.4}$$

where, ϕ_{MS} is the metal-semiconductor work function, ϕ_F is the Fermi-potential of the bulk, Q_D is the average depletion charge density, and Q_{SS} is the trapped charge density inside the gate oxide. The average depletion charge per unit gate area can be further expressed as

$$Q_D = (W)(L)\left(\sqrt{2\varepsilon_{Si} q N_{SUB}}\right) \tag{2.5}$$

where, N_{SUB} is the substrate doping density. It can be seen from Equations (2.3) through (2.5) that mismatches during fabrication will cause

i. Mismatch in the threshold voltage of the devices.

ii. Mismatch in β.

iii. And, finally mismatch in the drain current.

All of them are described next.

i. Threshold voltage mismatch.

The variance of the threshold voltage mismatch can be expressed as [2]

$$\sigma_{V_T}^2 = \frac{A_{1V_T}^2}{WL} + \frac{A_{2V_T}^2}{WL^2} - \frac{A_{3V_T}^2}{W^2 L} \tag{2.6}$$

For smaller values of L, the second term in R.H.S of Equation (2.6) will cause a large variance in threshold voltage. The third term in R.H.S of this equation will cause a reduction in the variance of the threshold voltage with increasing channel width.

In general, it is found that the effect of the second term is much larger than the third term when the geometries are varied. Thus, it can be summarized that

a) For large values of W and L, the variance of the threshold voltage reduces to

$$\sigma_{V_T}^2 = \frac{A_{1V_T}^2}{WL} \propto \frac{1}{area} \tag{2.7}$$

b) For large W and extremely small channel lengths, the variance of the threshold voltage becomes

$$\sigma_{V_T}^2 = \frac{A_{2V_T}^2}{WL^2} \propto \frac{1}{L^2} \tag{2.8}$$

Generally, the standard deviation of the threshold voltage mismatch is inversely proportional to square root of the device area. In [7], based on experimental results with smaller channel lengths, it was found to vary inversely with $[area]^{3/4}$. The smallest threshold voltage mismatch can be obtained for large L and small W. But this condition may not be suitable for the design requirements where mostly higher aspect ratios (W/L) are needed for larger transconductances. In [4], it is suggested that the threshold voltage mismatch can be optimized using the condition $\frac{W_{drawn}}{L_{drawn}} = \frac{DW}{DL}$ where DW and DL are the lateral out-diffusions along the channel width and the channel length respectively during processing. This condition will make the aspect ratios for the transistors constant, and it might not agree with the design requirements.

ii. β mismatch: β can be expressed as

$$\beta = \mu C_{OX} \frac{W_{eff}}{L_{eff}} \tag{2.9}$$

The variation in β is primarily caused by variations in the mobility and the device dimensions. The effect of mobility variation (caused by dopant variation) is the most dominant. In general, β mismatch follows the same trend as the threshold voltage mismatch.

iii. Drain current mismatch.

In [9], the relationship between drain current mismatch and mismatches in V_T and β was derived as

$$\frac{\sigma^2(\Delta I_D)}{I_D} = \frac{\sigma^2(\Delta\beta)}{\beta^2} + 4\frac{\sigma^2(\Delta V_T)}{(V_{GS} - V_T)^2} \tag{2.10}$$

Mismatch in drain current will result in "systematic offset". The improvement in drain current matching requires improved matching for both V_T and β. The conditions for better V_T and β matching are the same: larger channel lengths have better matching than smaller channel lengths, and larger device area improves matching.

There is another aspect of matching related to back-gate bias for MOS transistors in weak inversion [3,5]. The source-to substrate bias can play an important role in matching of the drain current. The minimum feature size studied in [3,5] was 1.2 μm. In this study, the following were shown for weakly inverted MOS devices through experimental data:

a) Reversed-biased source-to-substrate junction degraded matching in the drain currents.
b) Forward biased source-to-substrate junction improved matching of the drain currents.

This study showed that forward biasing the bulks can yield better matching, but it imposes problems of latch-up, and the magnitude of forward-biased current through the source-to-bulk diodes need to be controlled for proper circuit operation. The actual matching performance of different device geometries can be studied through experimental data as done in [2-10]. It can also be studied through design for different channel lengths.

When designing circuits using minimum feature-size channel lengths, the following conclusions can be drawn about matching,

- Small channel lengths worsen matching. With smaller channel lengths, the widths need to be made larger to achieve some improvement in matching due to larger device area. Larger widths will tend to make the device operate in weak inversion.
- Transistors, when operated in weak inversion can have improved matching with forward biasing of source-to-substrate junction diodes.

2.4 Limits on Supply Voltage

The current state of the CMOS technology has allowed tremendous downscaling in geometry, but it has also scaled down the limits of the power supply voltages. In most of the current CMOS processes, the maximum allowable supply voltage is less than 3 volts. Using a first-order approximation, the maximum supply voltage in a process can be approximated as 10 times the minimum feature size in that process. Application of higher supply voltages can result in higher reversed-biased diode junction voltages (like across the drain-substrate junction), and it can cause avalanche breakdown of the junctions. The gate oxide thickness has also decreased causing an increase in the electric field inside the oxide. For higher gate bias voltages, the electric field inside the gate oxide can exceed the maximum value of the critical electric field for oxide breakdown causing large tunneling gate current. With smaller channel lengths, the distribution of potential near the drain end becomes steeper, and the derivative of the potential (electric field) near the drain end is large. This causes hot carrier degradation due to the generation of hot electrons and holes. Thus, the performance of the smaller channel length devices will get degraded with technology scaling.

2.5 Noise

The limits of supply voltage are being scaled down with the scaling of the CMOS technology. The output swing levels of the circuits are dependent on the supply voltage, which are also getting scaled down with technology. For most of the analog circuits, dynamic range is an important specification. The upper limit of the dynamic range is dependent on the maximum output swing level, and the lower limit is dependent on the noise floor. Since the upper limit of the dynamic range is getting scaled down due to downscaling of the supply voltage, there is tremendous need to reduce the noise floor to achieve appreciable dynamic range. So, circuits designed in minimum channel lengths should have low noise. In CMOS circuits, the various sources of noise can be visualized as [11]

- Flicker or $1/f$ noise: This noise is due to the random generation and recombination of carriers at the $Si - SiO_2$ interface. The generation and recombination lifetime of these carriers is large, thus this kind of noise is very dominant in lower frequency, and it is negligible in higher frequencies. In a MOS transistor, flicker noise can be expressed as

$$\overline{i}_n^2 = \left(\frac{KF}{\frac{2K'WLC_{ox}}{f}} \right) \Delta f \qquad (2.11)$$

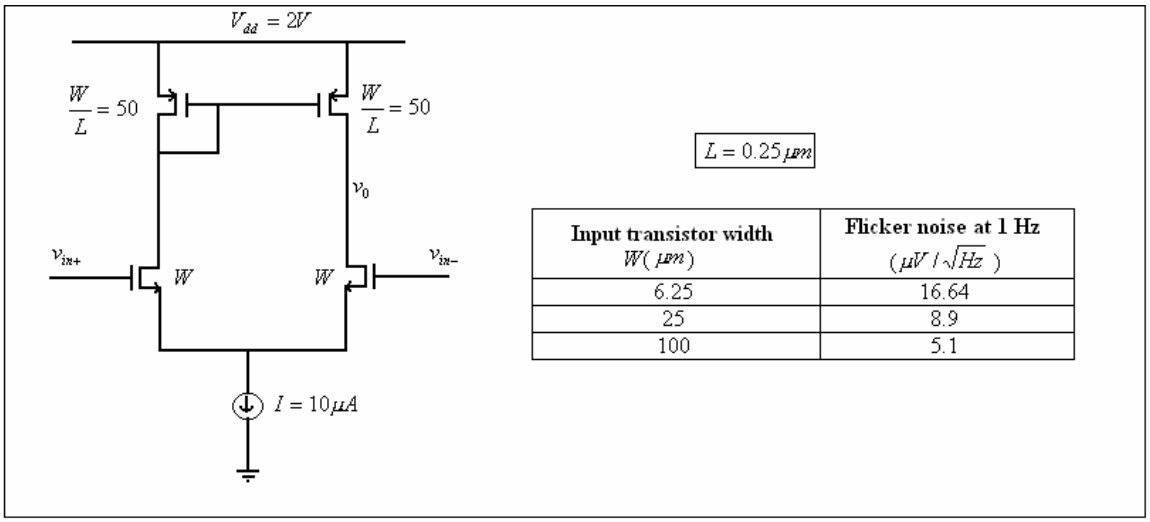
where, KF is the noise factor, and f is the frequency.

This is the dominant source of noise at low frequencies. With technology scaling, the values of K' and C_{ox} are increasing, which will lower the flicker

noise, but the use of smaller channel lengths will cause more noise due to decrease in area as suggested by Equation (2.11). So, when designing circuits at minimum channel length, larger widths should be used to reduce flicker noise. The flicker noise can also be reduced by switched-biased techniques [12-14]. If a switching pulse waveform is used to periodically switch the circuit from *on* to *off* state, then the flicker noise is present only in the *on* cycle when the carriers are present in the channel. In the *off* state, the channel is depleted of carriers, and the flicker noise is negligible. Using a 50% duty cycle of the switching waveform, the flicker noise can be reduced by a factor of 2. This technique is specially suited for oscillators whose phase noise can be reduced using this technique. In [12,13], it is also reported that larger reduction of the flicker noise can be achieved by turning *off* the device from strong inversion to strong accumulation. The reduction in the flicker noise is directly proportional to how much the device is pushed from inversion into accumulation. This reduction in the flicker noise is also inversely proportional to the switching frequency.

When using smaller channel lengths, the most viable way to reduce the flicker noise is to increase the width of the input transistors and maintain very high gain from the input to the output. Thus, the input stage will become the dominant source of noise, and the gain will reduce the noise contributions from various other elements in the following stages of the circuit. In Figure 2.7, simulation results for the flicker noise at 1 Hz are presented. The channel length of the devices was fixed at 0.25 μm . The widths of the input transistors

were varied to study their effect on the flicker noise. As expected, the flicker noise decreased with increase in the channel width.



Input transistor width $W(\mu m)$	Flicker noise at 1 Hz $(\mu V/\sqrt{Hz})$
6.25	16.64
25	8.9
100	5.1

Figure 2.7. Simulation results of the flicker noise at 1 Hz with varied input transistor widths.

ii. Thermal noise of the channel: Thermal noise is caused by the carriers in the channel. The channel acts as a resistor when inverted, and it gives rise to thermal noise. The classical noise model for drain thermal noise is given by

$$\overline{i_d}^2 = 4kT\gamma g_{d0}\Delta f \qquad (2.12)$$

where, $g_{d0} = (g_m + g_{mb} + g_{ds})$, and γ is a bias dependent parameter. $\gamma = 2/3$ in saturation and $2/3 < \gamma < 1$ in the triode region. This noise model is valid only for long channel devices. In small geometry devices, most of the carriers travel with saturation velocity, and they cause more thermal noise in the channel.

Various new thermal noise models have been proposed in [12,15,16] for smaller geometries, where the thermal noise was modeled as

$$\bar{i}_d^2 = 4kT \frac{\mu_{eff}}{L_{eff}^2} Q_{inv} \Delta f \tag{2.13}$$

where, μ_{eff} is the effective carrier mobility in the channel, Q_{inv} is the inversion channel charge per unit area, and $L_{eff} = L - \Delta L$. L is the channel length, and ΔL is the reduction in the channel length caused in saturation due to extension of the drain depletion region into the channel. In small channel length devices operated in saturation, the thermal noise in the channel is very large due to smaller value of L_{eff}. Much of the increase in noise may be attributed to large channel length modulation and drain-induced barrier lowering effects. The thermal noise in the channel can be kept low with smaller values of Q_{inv}, which will correspond to smaller drain currents. As reported in [11], using back gate reversed-biased technique, the thermal noise in the channel can be reduced for devices with small channel lengths and large widths. Experimental results also show that the thermal noise in the channel is directly proportional to the drain current [15].

iii. Gate resistance noise: This noise is due to the thermal noise generated by the gate resistance, which is caused by the finite gate contact resistance and finite sheet resistance of the gate material. The gate resistance (R_g) can be given by

$$R_g = \frac{R_{g,sq}}{3}\left(\frac{W}{L}\right) \tag{2.14}$$

where, $R_{g,sq}$ is the sheet resistance of the gate.

It is desired to have low sheet resistance and small aspect ratio to reduce the gate resistance noise. For MOS devices with polysilicide gates, this noise becomes insignificant.

iv. Induced gate noise: This noise is due to the thermal noise generated by the carriers in the channel, which capacitively gets coupled on to the gate as a gate current. This noise is highly correlated to the thermal noise in the channel. It is dependent on the value of the gate oxide capacitance. With shrinking technology, the gate oxide capacitance has increased, which has decreased the gate capacitive reactance. Thus, at lower frequencies, more capacitive coupling of thermal noise takes place from the channel to the gate. Smaller gate dimensions will reduce this noise effect due to reduction in the gate oxide capacitance, but this will tend to increase other noise effects.

In summary, the flicker noise can be reduced by using larger channel widths and switched-biasing techniques. Decreasing the drain current can reduce the thermal noise, but it will affect the circuit performance. The induced gate noise can be reduced with smaller device area, which generally is not a good choice.

2.6 High Frequency Performance

One of the major reasons for using smaller device dimensions is to achieve higher bandwidth. The bandwidth of a circuit is either limited by the external load capacitance, or the internal parasitic capacitances of the nodes. For smaller output load capacitances, decrease in the width and the length of the devices will cause a decrease in the parasitic capacitances, which will improve the bandwidth. In CMOS processes, a figure of high frequency limitation is given by the "*transition frequency*" parameter f_T, which is estimated as

$$f_T \cong \frac{g_m}{C_{gs}} \tag{2.15}$$

It is evident that f_T will increase as the device dimensions are scaled down because the transconductance of the MOS device increases with decrease in the channel length, which also causes a decrease in C_{gs}. Overall, from Equation (2.15), smaller channel lengths will result in a higher f_T.

2.7 Distortion

Distortion is an important performance specification in most of the analog circuits. It is often given by THD (total harmonic distortion), which is a ratio of the power in the fundamental component to the combined power of all the higher order harmonics of the non-linear circuit. The power in the fundamental component is dependent on the linear gain of the circuit. In CMOS circuits, this linear gain is often the product of g_m and r_{ds} of the MOS devices. Small channel length devices tend to show a linear transfer characteristics, i.e., their drain current varies almost linearly with the gate bias. This inherently makes the g_m almost constant with variations in the gate bias, which is an essential requirement for good distortion performance. On the other hand, smaller channel length devices have poor r_{ds} due to large channel length modulation effects, and it varies appreciably with change in V_{ds}. This has a major effect on the reduction of the linear gain of the circuit, and it strengthens the harmonics. This causes a decrease in the power of the fundamental frequency component, which in turn degrades the THD performance.

2.8 Summary of Use of Minimum Channel Lengths

Smaller channel lengths affect conventional DC biasing schemes. The limit on power supply is decreasing, and there is a need for new biasing schemes that can perform well with lower power supplies. Small-signal gain is an important specification, and large channel length modulation effects in smaller channel length devices heavily degrade it. Use of small channel lengths increase noise as well as mismatch. The distortion performance is also degraded with smaller channel length devices. Other than the bandwidth, almost all of the important performance specifications of the circuit are degraded due to the use of smaller channel lengths. Conventional circuit architectures will tend to fail when designed in minimum channel lengths, and there is a need to develop new design techniques suitable for minimum channel length designs.

The performance of the analog CMOS circuits is not only dependent on the channel length, but it is also dependent on the technology. Digital circuits are often scaled when moving from one technology to another, but scalability is a challenge for the analog circuits. The performance of the analog circuit is dependent on various parameters, which are dependent on the technology. In the following section, the dependence of the performance of the analog circuits on the technology is discussed.

2.9 Technology-Dependent Circuit Performance

The various implications of using small channel length devices were discussed in the previous sections. In this section, various aspects related to the dependence of the circuit performance on the technology are discussed. The drain current equation of a MOS transistor in saturation is given by

$$I_D = K' \frac{W}{L} \frac{(V_{GS} - V_T)^2}{2} (1 + \lambda V_{DS}) \tag{2.16}$$

Equation (2.16) is valid only for long channel length devices, and it is an approximation for smaller channel lengths. In this equation, K', V_T, and λ can be seen as the *technology-dependent* parameters. Across different technologies, these 3 parameters will vary causing a change in the drain current. This will change the biasing conditions of the circuit and affect the circuit performance.

The objective of the research in this thesis is to develop circuits whose performance is insensitive to the technology as well as the channel length. The drain current is dependent on the *technology-dependent* parameters. Also, for smaller channel lengths, the drain current given by Equation (2.16) is an approximation. Various drain current models for short channel lengths have been proposed; the most popular being the BSIM models [17]. For simplicity, the drain current equation for long channel devices is given by Equation (2.16) where

$$I_D \propto (V_{GS} - V_T)^2 \tag{2.17}$$

For small channel length devices, the drain current can be approximated as

$$I_D \propto (V_{GS} - V_T) \tag{2.18}$$

It can be concluded that the drain current is not only dependent on the *technology-dependent* parameters but also on the channel length. To develop a scalable architecture, the circuit performance needs to be made independent of the design equations, because these equations are sensitive to both the *technology-dependent* parameters as well as the channel length. A unified approach needs to be developed that will yield technology as well as channel length insensitive circuits. One way to achieve this is by expressing the performance specifications of the circuit as ratios, which will result in the same performance across different technologies as well as channel lengths.

In the following chapters, the design of technology-independent op amps with all small channel length devices will be discussed. The op amp has been chosen as an example circuit to study scalability and the impact of small channel lengths. In the following sections, some sample simulations of two commonly used op amp topologies will be presented for understanding the affect of the technology on the circuit performance.

2.9.1 Op Amp with Current-mirror Load

A simple, two-stage, Miller-Compensated op amp is shown in Figure 2.8. It is one of the most widely-used versions of the op amp. In this section, the performance of this circuit will be verified across two different CMOS technologies. The importance of this exercise is to understand the effect of *technology-dependent* parameters on the circuit performance. . If the transistors of this op amp were scaled as-it-is into different technologies, then its performance will be affected. Simulations were performed on this op amp in a 0.25 μm CMOS and a 0.18 μm CMOS technology. The same circuit (with the same device sizes) was used in both the technologies. Their performance is compared in Table 2.2.

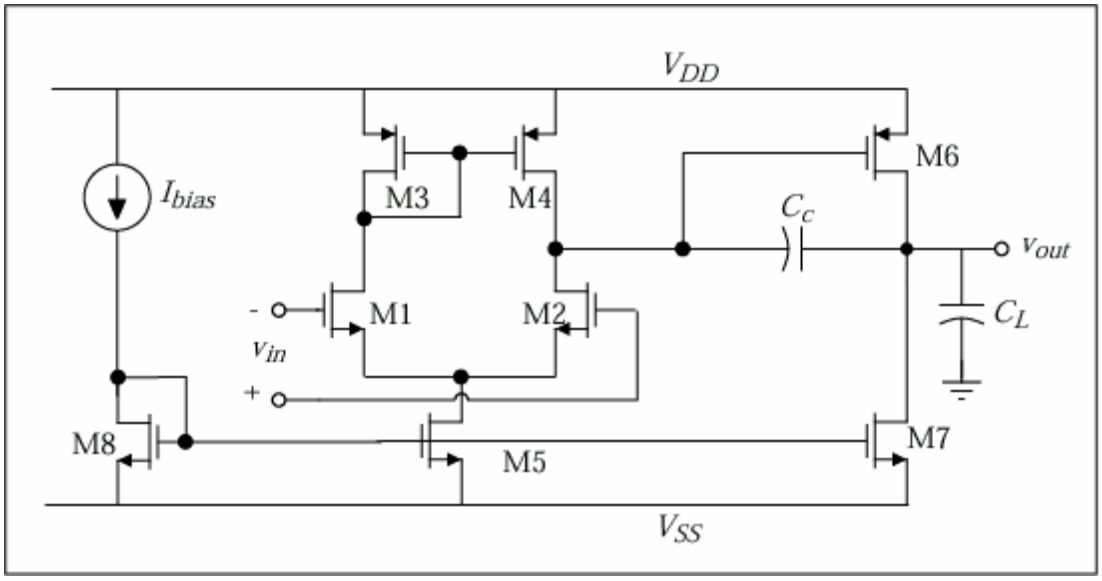


Figure 2.8. Two-stage op amp with current mirror load

Table 2.1. Component values for the two-stage op amp with current mirror load

Parameter	Value
I_{bias}	10 μA
$S_1 = S_2 = (0.5)S_5 = (0.5)S_8$	10
$S_3 = S_4$	10
S_6	100
S_7	100
C_C	0.5 pF
C_L	1 pF

$* S_i = \left(\frac{W}{L}\right)_i$

The performance comparison of the two-stage, Miller-compensated opamp in two CMOS technologies is shown next. The channel length of all the devices was kept the same at 1 um in both the technologies, and the same aspect ratios were maintained in both of them. This simulation exercise was merely to study the effect of the technology on the circuit performance, and it was not aimed at studying the effect of small channel length devices. It can be seen that most of the performance specifications of the op amp changed in both the technologies. The value of A_v remained relatively large in both of them. The UGBW frequency changed, but the phase margin remained almost the same. In general, both the

UGBW frequency and the phase margin can change, and the circuit, which was stable in one technology, can become unstable in the other. The overall performance of the op amp will vary across different technologies.

Table 2.2. Comparison of the simulated performance of the two-stage op amp with current mirror load in two different CMOS technologies

Performance specification	**Simulated value**	
	0.25 μm CMOS	**0.18 μm CMOS**
Vdd	2 V	1.5 V
A_v	83 dB	77 dB
UGBW (CL= 1 pF)	20 MHz	27.5 MHz
Phase margin	45 deg	43 deg
Slew rate (CL= 1 pF)	+20, -16 $V / \mu s$	+22, -18 $V / \mu s$
ICMR	0.28 – 1.9 V	0.13 – 1.44 V
CMRR	81 dB	73 dB
PSRR	83 dB	79 dB
Input referred noise	8.2 $\mu V / \sqrt{Hz}$ (1 Hz) 20 $nV / \sqrt{Hz}$ (1 MHz)	3.5 $\mu V / \sqrt{Hz}$ (1 Hz) 18 $nV / \sqrt{Hz}$ (1 MHz)
Idd	73 μA	76 μA

2.9.2 Cascode Op Amp

Similar to the two-stage, Miller-compensated op amp, a cascode op amp is being investigated in this section for technology-dependent performance. The cascode op amp is shown in Figure 2.9. The component values are shown in Table 2.3. If the transistors of this op amp were scaled as-it-is into different technologies, then its performance will be affected. Simulations were performed on this op amp in a 0.25 μm CMOS and a 0.18 μm CMOS technology. The same circuit (with same device sizes) was used in both the technologies. Again, this simulation exercise was to verify technology dependence on the circuit performance; it was not aimed at studying the effects of small channel lengths.

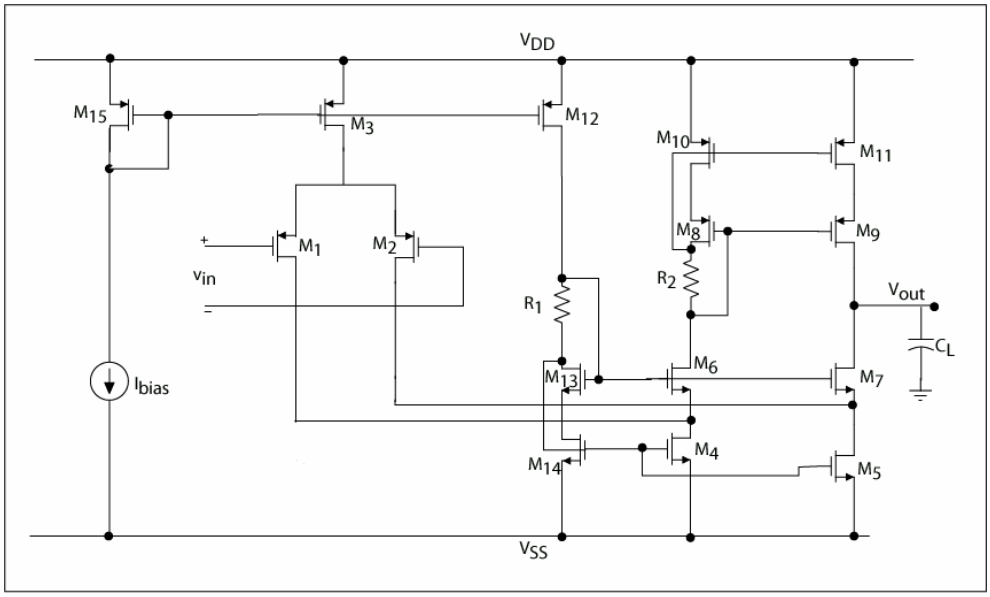


Figure 2.9. Cascode op amp

Table 2.3. Component values for the cascode op amp

Parameter	Value
I_{bias}	10 μA
$S_1 = S_2 = (0.5)S_3 = (0.5)S_{15}$	10
$S_{13} = S_6 = S_7 = S_{14} = S_4 = S_5$	100
$S_8 = S_{10} = S_{11} = S_9$	100
S_{12}	100
$R_1 = R_2$	2 $K\Omega$
C_L	1 pF

* $S_i = \left(\frac{W}{L}\right)_i$

The simulation results for the cascode op amp are shown in Table 2.4. The same circuit was simulated in both the technologies. It can be seen that the performance of the op amp does vary with change in technology, especially the UGBW frequency is affected the most. But, this op amp architecture seems to be less susceptible to change in technology than the two-stage op amp with current mirror load. The small-signal gain of the op amp was small because the architecture was not optimized for better gain. The stress in this exercise was to verify the effect of technology on the performance and not on the absolute value of the performance specifications in a particular technology.

Table 2.4. Comparison of the performance of the cascode op amp in two different CMOS technologies

Performance specification	**Simulated value**	
	0.25 μm CMOS	**0.18 μm CMOS**
Vdd	2 V	1.5 V
A_v	58 dB	54 dB
UGBW (CL = 1 pF)	6 MHz	8 MHz
Phase margin	80 deg	84 deg
Slew rate (CL = 1 pF)	+7.2, -6.5 $V / \mu s$	+8.1, -7.9 $V / \mu s$
ICMR	0.1 – 1.46 V	0.1 – 1.22 V
CMRR	63 dB	51 dB
PSRR	32 dB	31 dB
Input referred noise	37 $\mu V / \sqrt{Hz}$ (1 Hz) 115 $nV / \sqrt{Hz}$ (1 MHz)	18.45 $\mu V / \sqrt{Hz}$ (1 Hz) 101 $nV / \sqrt{Hz}$ (1 MHz)
Idd	168 μA	171 μA

2.10 Effect of Technology Scaling

The performance of analog integrated circuits is effected by the *technology-dependent* parameter. At this point, it is meaningful to investigated the scaling of different circuit parameters with CMOS technology. The values for some circuit parameters are shown in Table 2.5. These values are typical to the present-dat CMOS processes.

Table 2.5. Circuit parameters with technology scaling

Minimum Feature-size	**Nominal Power Supply**	**Gate-oxide Thickness**	**Threshold Voltage (NMOS)**
0.25 μm	2.5 V	5.5 nm	400 mV
0.18 μm	1.8 V	4.2 nm	300 mV
0.09 μm	1 V	2.5 nm	200 mV

As the technology scales, the gate-oxide thickness and the nominal power supply also scales almost linearly, but the threshold voltage does not scale linearly. A better way to visualize this effect is by normalizing these quantities with respect to the minimum feature-size, and such a plot is shown in Figure 2.10. In this plot, V_{DD}, t_{ox}, and V_T are normalized with respect to the minimum feature-size.

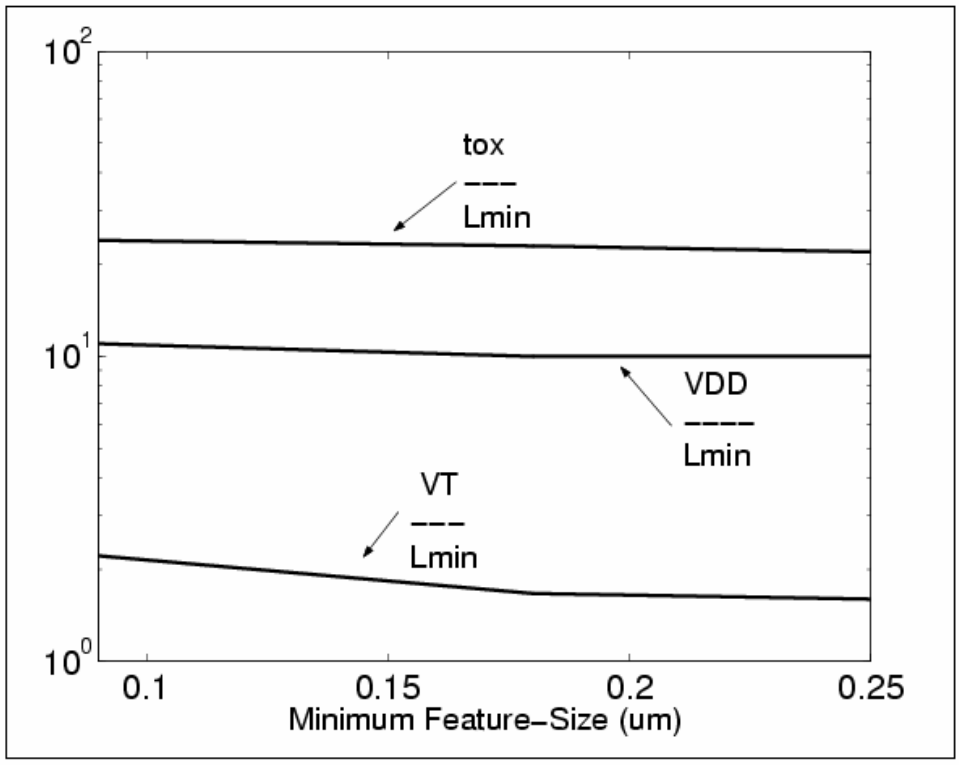


Figure 2.10. Normalized power supply, gate-oxide thickness, and threshold volatge with respect to minimum feature-size.

As it can be seen from Figure 2.10, both the oxide-thickness and the power supply scale linearly with the technology, but the threshold voltage does not follow this trend. One of the reasons why the threshold voltage can not be scaled linearly is because if its value is made too small, across process corners, an accumulation-mode device might become a depletion-mode device. It can be seen that the threshold voltage is actually more than its expected linearly-scaled value. This suggests that the power supply is getting scaled down faster than the threshold voltage, which will force the devices to operate in "poor" saturation with small V_{ds}. Moreover, with scaling of the channel length, the Early voltages are

degrading at a rate larger than the linear rate. This would put even more stress on the circuit techniques to design for large small-signal gains. Since one of the objectives of this research is to develop analog integrated circuits with minimum channel length devices, boosting the small-signal gain will become an important concern. In the next sections, the design of high small-signal gain stages is discussed. These gain stages use a small-signal negative resistance scheme to boost up the small-signal output resistance and gain while using all minimum feature-size channel length transistors.

2.11 $L_{\min}$ -based Gain Stage with Constant Gain

The impediments in designing analog CMOS circuits at minimum feature size channel length ($L_{\min}$), and the technology-dependent performance of these analog circuits were discussed in the previous sections. In order to develop circuits with technology-independent performance with $L_{\min}$-based devices, the performance should be made insensitive to both the technology and the channel length. In this thesis, the operational amplifier (op amp) is chosen as an example of study. The design of a single, $L_{\min}$-based gain stage, which will be a part of a two-stage op amp, is discussed in this section.

One of the most important performance specifications of an op amp is its small-signal voltage gain (A_V). When using $L_{\min}$ as the channel length for the devices, the value of A_V decreases largely due to large values of λ_N and λ_P

caused by large channel-length modulation effects. In most applications, unless the op amp has a satisfactory gain ($A_V \geq 60$ dB), it doesn't qualify as a good op amp (ideally the gain should be infinity). In $L_{\min}$-based op amps using conventional techniques, to achieve high overall gain, more than two gain stages need to be cascaded, which will make the compensation of the op amp very challenging and complicated (due to larger number of poles). When using $L_{\min}$ as the channel length, the output nodes tend to become low impedance nodes due to large values of λ_N and λ_P, which degrades the value of A_V. The variation in the value of A_V for different channel lengths was shown in Figure 2.6. In the following sections, two gain stage architectures with all $L_{\min}$ based devices are developed.

Different gain-boosting schemes have been reported in the literature [18]–[32]. These gain-boosting techniques can be widely classified into two groups:

1. Gain-boosting in the regulated cascode topology [18]-[26], which uses negative feedback to boost the transconductance of one of the output transistors of the cascoded output structure. This scheme is only applicable to cascoded op amps, and it can give large gain even with the use of minimum channel length devices. But, due to large number of poles and zeros, the compensation in this technique is dependent on the technology as well as on the channel length.

2. Gain boosting using positive feedback [27]-[32], where a small-signal negative resistance is used to cancel the positive output resistance, resulting in high-impedance outputs. In this research, this technique is used to generate two high-gain stages, and the first architecture of an $L_{\min}$ based gain stage is shown in Figure 2.11. In this gain stage, the value of A_V can be expressed as a ratio of two NMOS transconductances (g_m). Even though the absolute values of the two g_ms will be dependent on the channel length and the technology, their ratio can be made constant across different technologies and channel lengths.

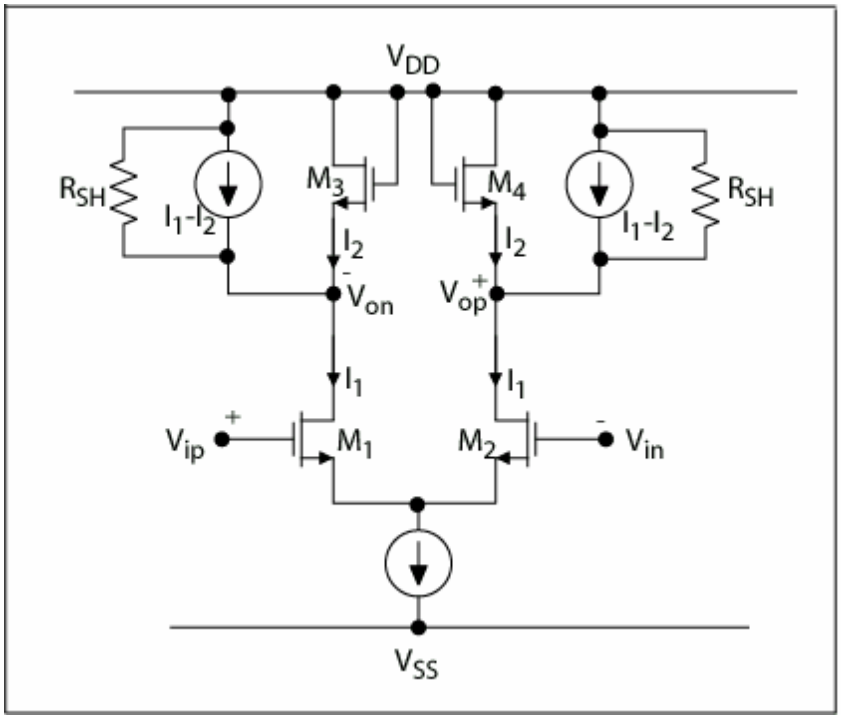


Figure 2.11. $L_{\min}$-based gain stage for constant gain

In Figure 2.11, M_1 and M_2 form the differential input stage, and M_3 and M_4 make up the "$1/g_m$" load stage (as the load seen at the output is inverse of the transconductance of the diode-connected NMOS device). Here, the differential voltage gain can be given by

$$A_V = \frac{g_{m1}}{\left(g_{m3} + g_{ds3} + g_{ds1} + 1/R_{SH} \right)} \tag{2.19}$$

where, R_{SH} is the shunt resistance associated with the current source $I_1 - I_2$. These ideal current sources can be implemented using PMOS transistors driven by a constant gate bias. In Equation (2.19), if the condition

$$g_{m3} >> \left(g_{ds1} + g_{ds3} + 1/R_{SH} \right) \tag{2.20}$$

can be achieved, then we will have

$$A_V \cong \frac{g_{m1}}{g_{m3}} \tag{2.21}$$

or, $$A_V = \sqrt{\left(\frac{W_1}{L_1}\right)\left(\frac{L_3}{W_3}\right)\left(\frac{I_1}{I_2}\right)} \quad \text{in moderate/strong inversion} \tag{2.22}$$

and $$A_V = \left(\frac{I_1}{I_2}\right) \quad \text{in weak inversion} \tag{2.23}$$

The expression for A_V, given by Equation (2.22), is true only for long channel length transistors. It can only be used as an approximation for smaller channel length devices. If the devices are operated in weak inversion, then Equation (2.23) will represent the small-signal gain for both small as well as long channel length devices. Thus, the small-signal voltage gain can be expressed as ratios of

geometries and/or currents. In order to achieve a large value for A_V, $g_{m3} << g_{m1}$. Let us assume that

$$g_{m1} \cong 100 g_{m3}.$$

This will give A_V of 100, but the values of g_{ds1} and R_{SH} will tend to become comparable to g_{m3} because $g_m / g_{ds} \cong 100$ for longer channel lengths and even lesser for shorter channel lengths. Thus, the required condition in Equation (2.20) will not be satisfied, and A_V will depend on both g_m as well as g_{ds} values.

The conductance (g_{ds}) terms in Equation (2.19) at the output nodes can be cancelled using appropriate small-signal negative conductances, and the resistance at the output nodes can be increased using a controlled negative resistance generation circuit connected at the output of the gain stage. The generation of the negative resistance should be such that the effective output resistance always remains positive. A modified version of the gain stage in Figure 2.11, which uses the concept of small-signal negative resistance, is shown in Figure 2.12. It uses a small-signal, negative resistance circuit to cancel the positive g_{ds} terms in the denominator of Equation (2.19).

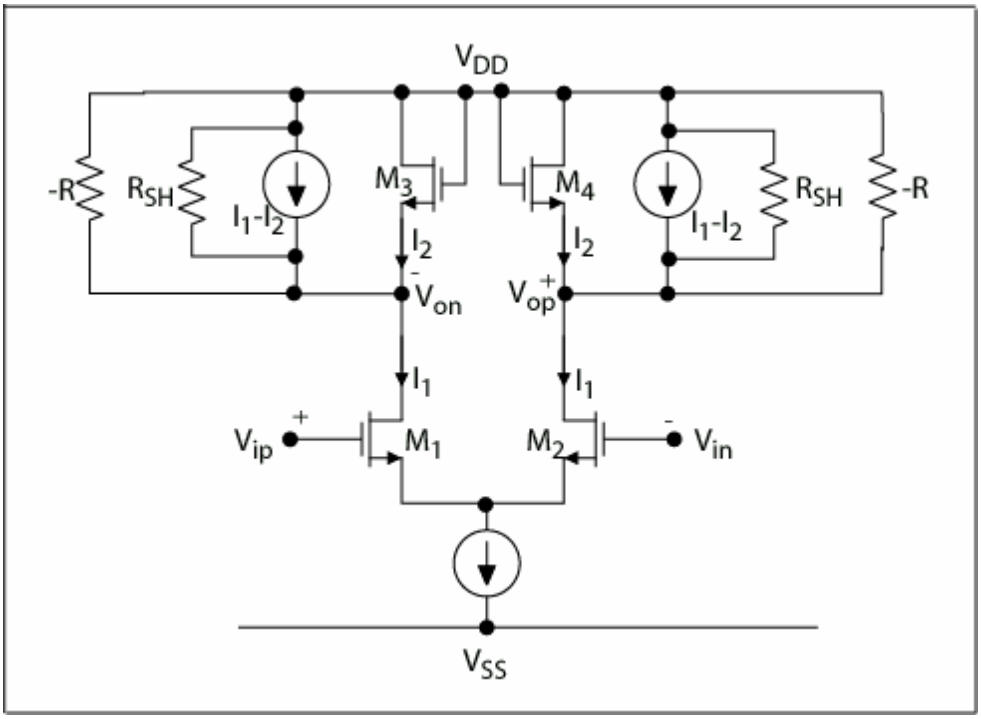


Figure 2.12. $L_{\min}$ -based gain stage with negative resistance

Using a controlled negative resistance generation scheme, the value of the negative resistance $(-R)$ needs to be set such that

$$(-1/R) \cong \left(g_{ds1} + g_{ds3} + 1/R_{SH}\right) \tag{2.24}$$

If the condition given by Equation (2.24) can be achieved, the small-signal voltage gain will become

$$A_V = \frac{g_{m1}}{\left(g_{m3} + g_{ds3} + g_{ds1} + 1/R_{SH} + 1/R\right)} \cong \frac{g_{m1}}{g_{m3}} \tag{2.25}$$

Thus, the small-signal gain can be expressed as the ratio of two, similar NMOS transconductances, whose absolute values can vary across different technologies and channel lengths, but their ratio will remain constant across them.

2.12 $L_{\min}$ -based Gain Stage for Maximum Gain

The circuit shown in Figure 2.12 can be designed to achieve a constant A_v. But, the same circuit can also be modified to achieve even larger A_v. If the entire positive conductance at the output were cancelled by a suitable negative conductance, the output resistance will tend to become infinite, thus yielding the maximum possible value of A_v for a fixed bias current. But, it is also important that the total output impedance should be positive. The modified version of Figure 2.12 is shown in Figure 2.13, where the "1/ g_m" load stages are removed.

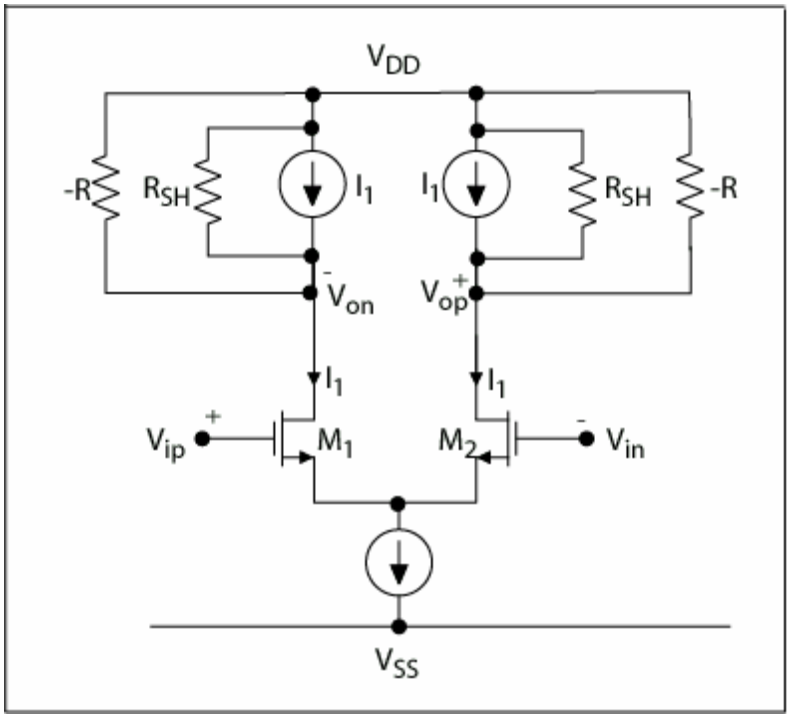


Figure 2.13. Modified gain stage for maximum gain

In Figure 2.13, the current source loads can be implemented using PMOS transistors. The input transconductance is g_{m1}. The output conductance can be given by

$$G_{out} = \left(g_{ds1} + \frac{1}{R_{SH}} + \frac{-1}{R} \right) \tag{2.26}$$

If the value of the small-signal negative resistance (–R) can be set such that

$$\frac{-1}{R} = g_{ds1} + \frac{1}{R_{SH}} \tag{2.27}$$

Then, the value of G_{out} will tend to become zero. It is important that this value should be positive. The small-signal gain can be expressed as

$$A_v = \frac{g_{m1}}{G_{out}} \cong +\infty \tag{2.28}$$

This gain will be dependent on technology as well as the channel length because g_{m1} will vary across them. Even though the value of g_{m1} will vary, proper cancellation of positive and negative conductances will result in high impedance output nodes. Thus, very large small-signal gain can be achieved while using $L_{\min}$ based devices across different technologies. But, in this technique, it is important to ensure that the effective output resistance should always be positive. Drawing an analogy between the effective resistance and a closed-loop feedback system, an effective positive resistance is associated with a negative feedback loop, but an effective negative resistance will correspond to a positive feedback loop. These feedback loops are not visible in Figure 2.13, but they will be present when the negative resistance circuit is implemented using MOS transistors. If this effective resistance becomes negative, then the positive feedback will dominate

over the negative feedback, and the output nodes will swing towards the power supply rails, i.e., the positive output V_{op} will swing towards V_{DD}, and the negative output V_{on} will swing towards V_{SS}, or vice versa. This will cause one of the two NMOS transistors forming the differential input pair to operate in the triode region, which will make the small-signal gain very small. The feedback loop will adjust the operating points such that even though the effective feedback in the loop is positive, the loop gain of the positive feedback loop remains less than unity, which will not cause the circuit to oscillate. As it will be shown in the following chapters, the generation of the small-signal negative resistance is controlled, and it will never make the effective output resistance negative in nature.

As discussed earlier, while using small channel lengths, it is wise to use larger channel widths to maintain good matching and noise performance. Large channel widths can sometimes make the MOS device operate in weak inversion. In the next section, the operation of a MOS device at the threshold of weak inversion is described. From Figure 2.12 and Equation (2.25), the small-signal gain can be expressed as the ratio of two NMOS transconductances. If the devices were operated in weak inversion, the ratio of their transconductances can be expressed as the ratio of the quiescent currents through them, and this can make the small-signal gain insensitive to the technology as well as the channel length. In the following section, an attempt has been made to approximate the aspect ratio for which the device goes from strong to weak inversion for a constant bias current.

2.13 Weak Inversion Operation of the MOS device

The small-signal gain, given by Equation (2.25), can be represented as the ratio of two NMOS transconductances. Moreover, if the transistors operate in weak inversion, the ratio of the transconductances can be simplified as the ratio of two bias currents. Thus, with weakly inverted MOS devices, a constant value of the small-signal gain can be achieved by ensuring a constant ratio of the bias currents through the devices. In order to operate a MOS device in weak inversion for a given bias current, one needs to know the aspect ratio of the device so as to operate the device in weak inversion. One such estimation is presented next. In Figure 2.14, a constant current, I, is sunk into the NMOS transistor.

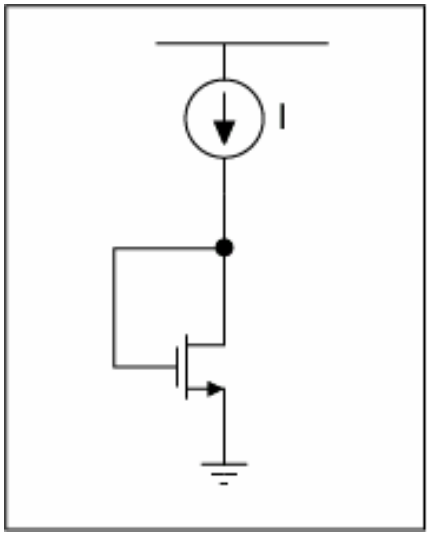


Figure 2.14. A constant current sunk into a diode-connected NMOS

If the NMOS device operates in strong inversion, the gate-to-source voltage can be given as

$$V_{GS} = V_T + V_{ds}(sat) \tag{2.29}$$

where,
$$V_{ds}(sat) = \sqrt{\frac{2I}{K'\left(\frac{W}{L}\right)}} \tag{2.30}$$

The above expression is true only for longer channel lengths, but it can be used as an approximation for smaller channel lengths. In Figure 2.14, if the bias current, I, is kept constant, and the aspect ratio of the NMOS device is increased, from Equation (2.30), the value of $V_{ds}(sat)$ will decrease till it starts to operate in weak inversion where these equations become invalid. As the aspect ratio is further increased, the area under the gate of the NMOS device increases causing the channel to become weakly inverted. The total current (or the inversion charge) in the channel is constant, but with increase in the channel area, the inversion charge per unit channel area decreases causing the channel to get weakly inverted. Thus, for a constant current, I, as the aspect ratio is increased, it is important to approximate the aspect ratio for which the MOS devices goes from strong inversion to weak inversion.

The threshold value of the aspect ratio for which the device makes a transition from strong inversion to weak inversion can be estimated by equating the drain current expressions in strong and weak inversion. The square-law expression for the drain current in strong inversion is valid only when the V_{GS} is almost 200 mV more than the threshold voltage. Thus, in the region

$V_T \leq V_{GS} \leq V_T + 0.2$ V, neither the square law (strong inversion), nor the exponential (weak inversion) behavior can alone represent the drain current, and using one or the other might lead to discontinuities in the drain current. Most of the present-day simulators use complicated smoothening functions to smooth the drain current in this transition region. In order for us to develop a simple estimate of the threshold value of the aspect ratio for weak inversion operation, we will equate the transconductances in strong and weak inversions. This technique of equating the transconductances will give an approximate solution because in the transition region, just like the drain current, the transconductances will also suffer from discontinuity. Nevertheless, we will still use this technique because it leads to a much simpler solution than equating the drain currents. Moreover, we only need an estimate rather than an accurate value of the aspect ratio. This technique is further explained with the help of Figure 2.15. In this figure, the transconductance of the MOS device is plotted as a function of its aspect ratio (W/L) for a fixed value of the drain current. The transition region separates the strong inversion region from the weak inversion region of operation. In the strong inversion region, the transconductance has square root dependence where as in the weak inversion region it is almost constant.

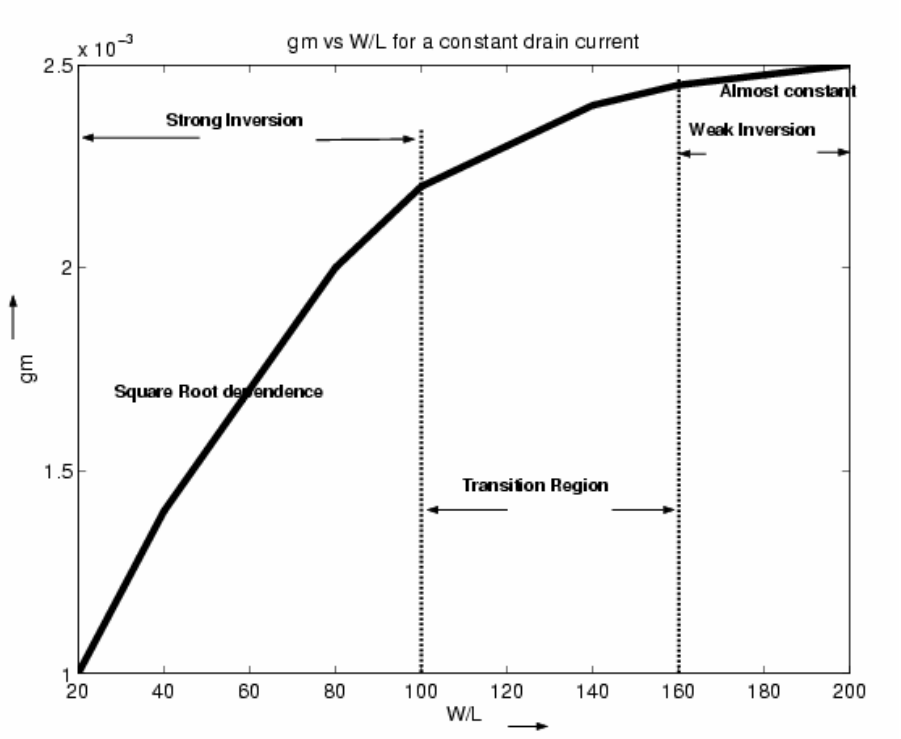


Figure 2.15. Variation of the MOS transconductance as a function of the aspect ratio for a fixed drain current.

The MOS transconductance in strong inversion can be given by

$$g_{m,strong} = \sqrt{2K'\left(\frac{W}{L}\right)I} \tag{2.31}$$

The square root dependence of g_m can be seen in Figure 2.14. The MOS transconductance in weak inversion can be given by

$$g_{m,weak} = \frac{I}{nV_t} \tag{2.32}$$

Equating the two transconductances given by Equations (2.31) and (2.32), we get

$$g_{m,strong} = g_{m,weak}$$

or, $$\sqrt{2K'\left(\frac{W}{L}\right)I} = \frac{I}{nV_t}$$

or, $$\left(\frac{W}{L}\right) = \frac{I}{2K'(nV_t)^2} \tag{2.33}$$

Equation (2.33) predicts the value of the aspect ratio for which the MOS device tends to enter into weak inversion for a constant bias current. V_t is the thermal voltage, and the value of n can be chosen as 2. The aspect ratio given by Equation (2.33) corresponds to a value in the transition region as shown in Figure 2.15. It does not accurately predict the threshold value of the aspect ratio, but it gives an estimate whose error will depend on the transition region. The validity of this assumption of equating the transconductances in strong and weak inversion, and the subsequent aspect ratio given by Equation (2.33) were verified through simulations. In these simulations, a constant current was sunk into a diode-connected NMOS device, and its V_{gs} was compared to its V_T reported by the simulator. From simulations, it was found that the aspect ratio given by Equation (2.33) resulted in V_{gs} that had an error of about 5 - 10 mV compared to the threshold voltage. In order to push the MOS device deeper into weak inversion, one can choose a larger value for the aspect ratio than the one given by Equation (2.33). Using this technique, if the MOS device is operated in weak inversion, the small-signal gain can be expressed as the ratio of two bias currents, which can easily be controlled for smaller channel length designs across different technologies.

2.14 Summary

It can be summarized that the performance of analog integrated circuits is affected by technology as well as channel length. The small and large signal parameters of the MOS transistors are dependent on the *technology-dependent* parameters, which vary largely across different technologies. Thus, when migrating from one technology to another, the aspect ratios need to be re-designed to maintain the desired performance. The channel length of the devices also affects the circuit performance. Circuit performance degrades with shrinking channel lengths. Thus, if the devices are scaled while migrating across different technologies, the circuit performance will depend on the scaled value of the device channel length, and most of the devices have to be re-designed for their aspect ratios to achieve the desired performance.

The small-signal gain is drastically reduced due to large channel length modulation effects in small channel length devices. To achieve large small-signal gain, two gain stages were developed in this chapter with all small channel length devices. The first gain stage uses a negative resistance scheme to cancel the MOS drain-to-source conductances at the outputs and represent the gain as the ratio of two similar NMOS transconductances. The absolute values of these transconductances can vary, but their ratio will remain constant and independent of the channel length and the technology. If the transistors are operated in weak inversion, the ratio of the transconductances can be expressed as the ratio of the bias currents through them. For a constant bias current, an estimate of the aspect ratio for which the device operates close to weak inversion was developed. The

second gain stage tries to achieve the maximum small-signal gain by the cancellation of the positive conductances and generating high impedance at the outputs. This architecture can be used to achieve the maximum possible small-signal gain for fixed bias currents. In this chapter, both of these gain stages were explained at the block level, and their transistor level implementation is described in the next chapter.

Chapter 3

CMOS Implementation of the Gain Stages in Minimum Channel Length

The implications of using small channel length devices on circuit performance were discussed in Chapter 2. It was seen that small channel lengths degrade small-signal gain, noise and matching among others. When performing $L_{\min}$ based design, one clever choice can be to use large device widths to achieve larger device area. As explained in Chapter 2, when using large device widths, for a given bias current, the transistor can be made to operate in weak inversion, and it can yield the maximum possible value of g_m, which will boost the value of A_v. Large device area will also decrease flicker noise and improve matching.

In this chapter, the circuit concepts shown in Figures 2.12 and 2.13 are implemented as CMOS circuits. A small-signal negative resistance generation circuit using MOS transistors is explained in the next section. It is integrated with a differential-in differential-out gain stage to achieve large small-signal gain. The consequence of bulk effects on the small-signal gain, and the operation of the common-mode feedback circuit are also discussed in the later sections.

3.1 Negative Resistance Circuit

As it was discussed in Chapter 2, gain boosting can be achieved using small-signal negative resistances [27]-[32]. Let us first try to develop the negative resistance generation circuit. Figure 3.1 shows a simple circuit to generate small-signal negative resistance.

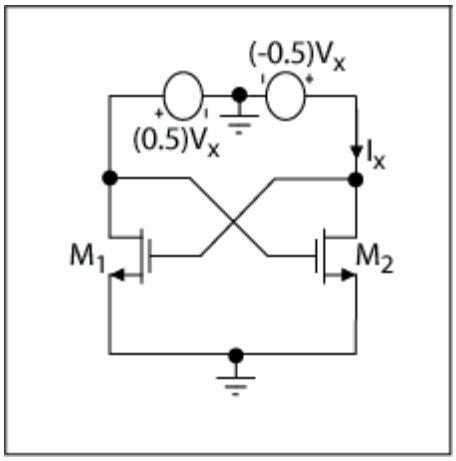


Figure 3.1. Negative resistance generation circuit

In Figure 3.1, the small-signal differential input voltage is applied as V_x. The small-signal voltages at the gates of M_1 and M_2 are given by

$$V_{gs1} = (-0.5)V_x \text{ and } V_{gs2} = (0.5)V_x$$

The small-signal current I_x can be given by

$$I_x = I_{d2} = \frac{g_{m2}}{2} V_x \tag{3.1}$$

Thus, the small-signal differential resistance is given by

$$R_x = \frac{V_x}{-I_x} = -\frac{2}{g_{m2}} \tag{3.2}$$

The value of the negative resistance as given by Equation (3.2) is dependent on g_m. But, from Equations (2.24) and (2.27), the negative conductance should cancel g_{ds} terms. The circuit shown in Figure 3.1 can be modified such that the negative conductance is dependent on g_{ds} rather than g_m, and it is shown in Figure 3.2.

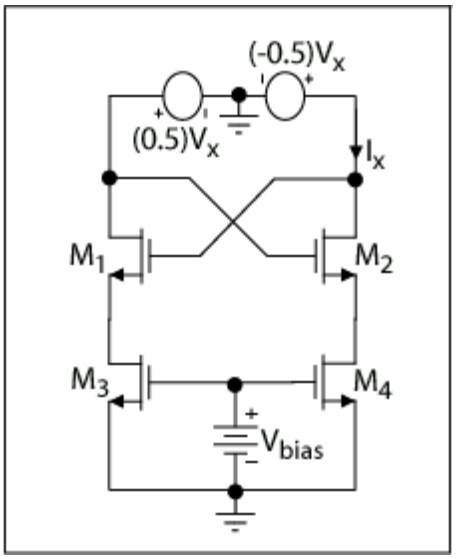


Figure 3.2. Modified negative resistance generation circuit

In Figure 3.2, the sources of M_1 and M_2 are degenerated by M_3 and M_4 respectively. If it is assumed that M_1 and M_2 act as ideal source followers ($g_m r_{ds} >> 1$ and the source follower gain $A_f \cong 1$ for these transistors), then Equation (3.3) can be modified as

$$R_x = \frac{V_x}{-I_x} = \frac{V_x}{-I_{d4}} = -\left[\frac{V_x}{A_f (0.5) V_x g_{ds4}}\right] \tag{3.3}$$

or, $$R_x = -\frac{2}{g_{ds4}} = -\left(\frac{1}{g_{ds3}} + \frac{1}{g_{ds4}}\right) \tag{3.4}$$

This way, the negative conductance, which now depends on g_{ds} terms, can be used to cancel the positive conductances at the output nodes of the differential gain stage. But, in reality, the gain of the MOS source followers is always less than unity ($A_f \leq 1$). So, Equation (3.4) can be modified as

$$R_x = \frac{V_x}{-I_x} = \frac{V_x}{-I_{d4}} = -\left[\frac{V_x}{A_f(0.5)V_x g_{ds4}}\right] \tag{3.5}$$

where, $A_f = \left(\frac{g_{m2}}{g_{m2} + g_{ds4}}\right) = \left(\frac{g_{m1}}{g_{m1} + g_{ds3}}\right)$ (3.6)

or, $R_x = -\frac{2}{A_f g_{ds4}} = -\frac{1}{A_f}\left(\frac{1}{g_{ds3}} + \frac{1}{g_{ds4}}\right)$ (3.7)

Thus, the value of the negative resistance becomes slightly larger in magnitude than the ideal value given by Equation (3.4). As it will be shown in the later sections, this will become an important practical limitation that will ensure a positive finite resistance at the output nodes. This finite positive output resistance will also cause a decrease in the value of A_v as it will cause an increase in the denominator terms of Equations (2.25) and (2.28).

3.2 Gain Stage with Negative Resistance and Constant Gain

The $L_{\min}$-based, differential-in differential-out gain stage is shown in Figure 3.3. All the devices have minimum feature-size channel length, and large values of λ_N and λ_P will result in small value of A_v. In this figure, the inclusion of M_6 is mainly because of proper biasing requirements, and it serves no other special purpose.

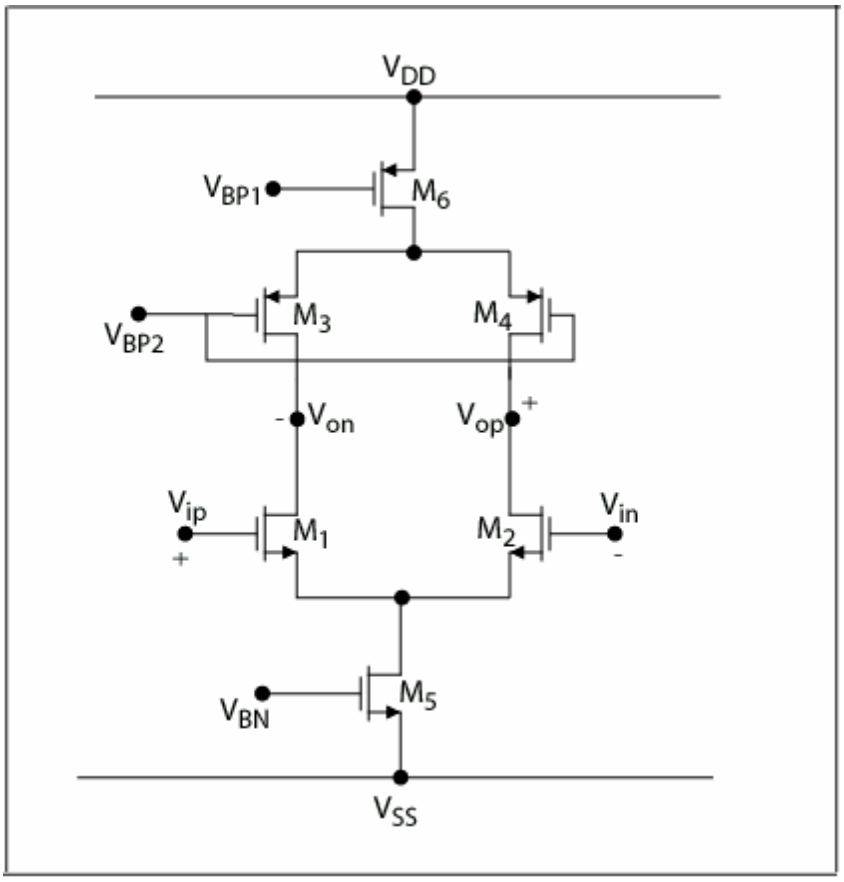


Figure 3.3. Differential-in differential-out gain stage

In Figure 3.3, the value of the small-signal gain can be given by

$$A_v = \frac{(V_{op} - V_{on})}{(V_{ip} - V_{in})} = \frac{g_{m1}}{g_{ds1} + g_{ds3}} = \frac{g_{m1}}{(\lambda_1 + \lambda_3) I_1} \tag{3.8}$$

When using $L_{\min}$ based devices, large values of λ_1 and λ_3 will degrade the value of A_v. As explained earlier in Chapter 2, the gain and the output impedance can be increased using a negative resistance scheme (shown in Figures 2.12 and

2.13). The implementation of the circuit technique in Figure 2.12 is shown next in Figure 3.4.

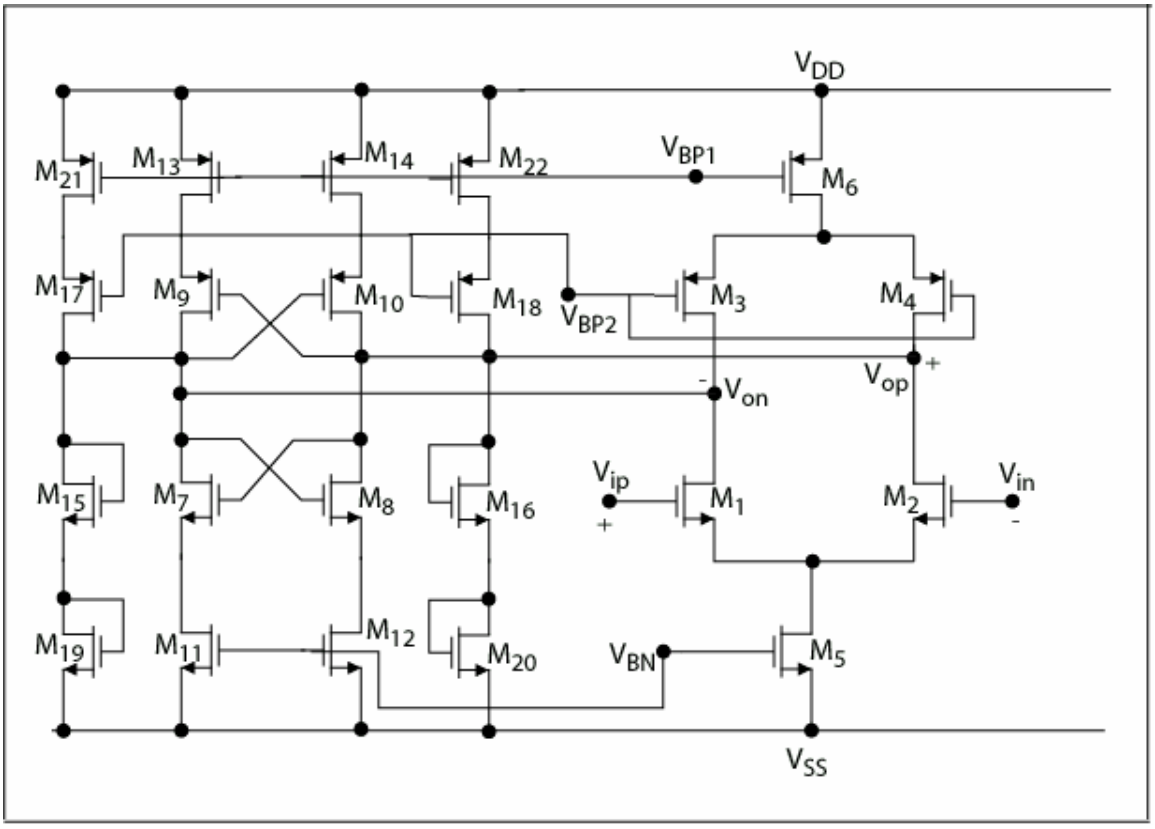


Figure 3.4 CMOS implementation of the gain stage with constant gain

Table 3.1. Aspect ratios of the transistors of the gain stage with constant gain

$S_1 = S_2 = (0.5)S_5 = S_7 = S_8 = S_{11} = S_{12}$	500X
$S_3 = S_4 = (0.5)S_6 = S_9 = S_{10} = S_{13} = S_{14}$	1000X
$S_{15} = S_{16} = S_{19} = S_{20}$	5X
$S_{17} = S_{18} = S_{21} = S_{22}$	10X

* $S_i = \left(\frac{W}{L}\right)_i$

In Figure 3.4, the transistors M_1 through M_6 constitute the differential-in differential-out gain stage; M_7 through M_{14} make up the small-signal negative resistance generation circuit; and M_{15}, M_{16}, M_{19}, and M_{20} make up the "$1/g_m$" load stage. As it can be seen in Figure 3.4, the "$1/g_m$" load stage actually generates a "$2/g_m$" loading at the output nodes. The design of the biasing voltages V_{BP1}, V_{BP2}, and V_{BN} will be shown later in this chapter. The aspect ratios of the transistors are given in Table 3.1; they are expressed as a multiple of $L_{\min}$, which is referred as "X" in the table. The value of the transistor width for operation in weak inversion was calculated using Equation (2.33). In order to make the devices operate into deeper weak inversion, their aspect ratios were made 5 times the value obtained from Equation (2.33), and they are quoted in Table 3.1. This made the g_m of the devices proportional to their bias current.

Due to the choice of the equal aspect ratios of the devices, the bias currents can be given as

$$I_1 + I_7 = I_3 + I_9 \text{ and } I_2 + I_8 = I_4 + I_{10} \tag{3.9}$$

Under nominal input common-mode voltage, assuming there are no mismatches in the currents, the bias currents can be written as

$$I_1 = I_3 = I_7 = I_9 \text{ and } I_2 = I_4 = I_8 = I_{10} \tag{3.10}$$

To understand the cancellation of positive and negative conductances at the output, a simple small-signal conductance-based model, derived from Figure 3.4, is shown in Figure 3.5. It constitutes the small-signal positive and negative conductances at the outputs.

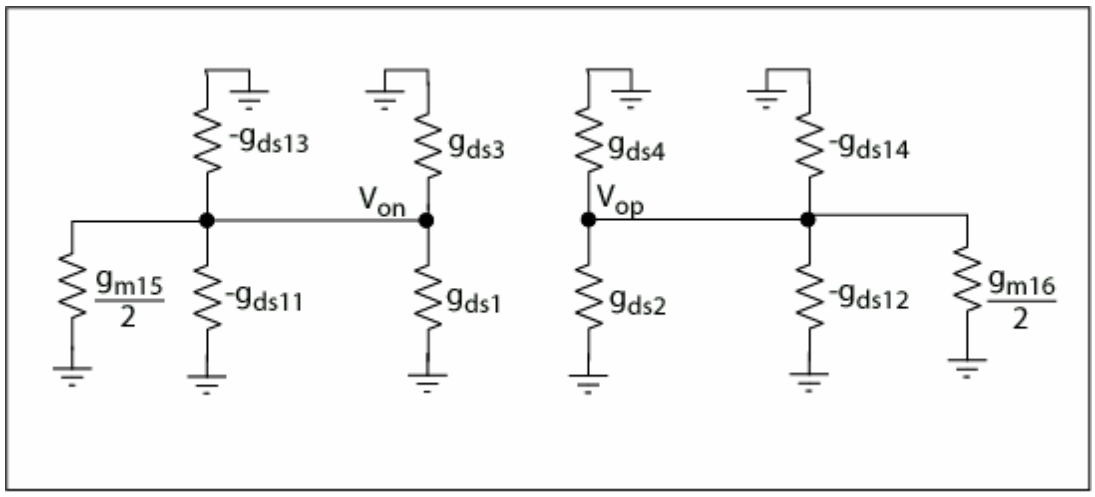


Figure 3.5 Small-signal conductance based model for the gain stage with constant gain

Considering the positive output node, the total conductance can be given by

$$G_{op} = (g_{ds2} + g_{ds4}) - (g_{ds12} + g_{ds14}) + \frac{g_{m16}}{2} \tag{3.11}$$

or, $$G_{op} = I_2(\lambda_2 + \lambda_4) - I_{12}(\lambda_{12} + \lambda_{14}) + \frac{g_{m16}}{2} \tag{3.12}$$

As it will be discussed in the next section, bulk effects tend to change the value of λ. But, for the time being, if we ignore the bulk effects on the values of λ, we will get

$$G_{op} = \frac{g_{m16}}{2} \tag{3.13}$$

Similarly, the total conductance at the negative output node can be given by

$$G_{on} = \frac{g_{m15}}{2} \tag{3.14}$$

Thus, the small-signal gain can be expressed as

$$A_v = \frac{g_{m2}}{G_{op}} = 2\frac{g_{m2}}{g_{m16}} = 2\frac{I_2}{I_{16}} \tag{3.15}$$

Using the aspect ratios from Table 3.1, the value of A_v will be 200. It can be seen that even if the absolute values of the bias currents vary, their ratio will remain constant. The same can be argued for different channel lengths and technologies. Although Equation (3.15) shows that A_v can be expressed as the ratio of two similar transconductances/currents, in reality, the value of A_v will depend on other factors, and it will be less than its ideal value given by Equation (3.15). One such factor was explained earlier using Equation (3.7) where a finite positive conductance always appears at the outputs due to the non-ideal MOS source followers. Another such factor affecting A_v is due to the bulk effects, which is discussed next.

3.3 Bulk Effects

Referring to Figure 3.4, considering the transistors M_4 and M_{14}, M_4 suffers from bulk effect ($V_{BS} \neq 0$) where as M_{14} does not have any bulk effect ($V_{BS} = 0$). The source-to-substrate junction of M_4 is reversed biased; this increases the threshold voltage of M_4, and it will consequently decrease the value of its saturation voltage, $V_{ds4}(sat)$. This decrease in the saturation voltage will cause an increase in its λ. The Id-Vds characteristics of two transistors, one with bulk effect and the other without bulk effect, are shown in Figure 3.6. The

value of the channel length modulation parameter, λ, can be determined by the slope of the drain current in the saturation region. The larger this slope is, the higher is the value of λ.

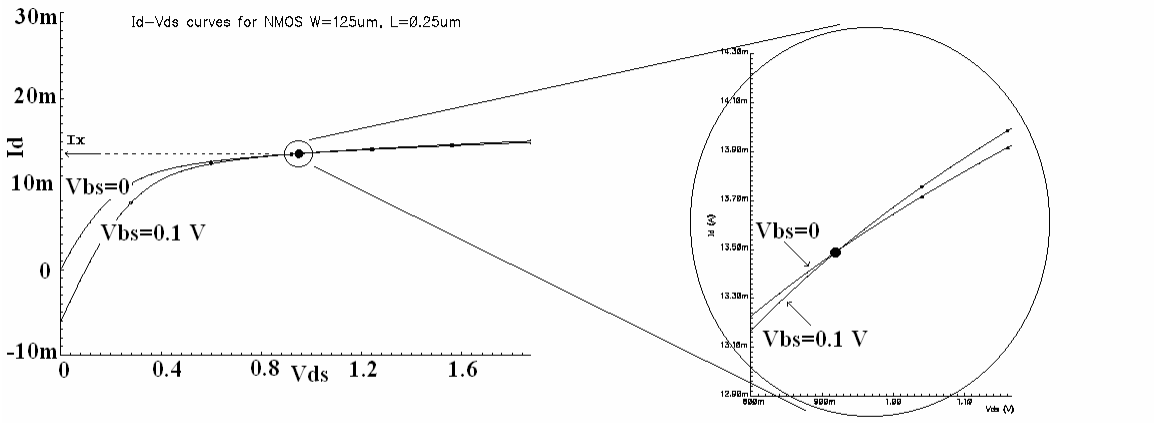


Figure 3.6. Bulk effect on the drain current

From Figure 3.6, for a constant value of the drain current, the transistor with bulk effect showed a steeper slope of the drain current, and this will give a larger value of λ. So, Equations (3.13), (3.14) and (3.15) can be modified as

$$G_{op} = I_2(\lambda_2 + \lambda_4) - I_{12}(\lambda_{12} + \lambda_{14}) + \frac{g_{m16}}{2} \tag{3.16}$$

or, $$G_{op} = I_2\{(\lambda_2 + \lambda_4) - (\lambda_{12} + \lambda_{14})\} + \frac{g_{m16}}{2} \tag{3.17}$$

where, due to bulk effects, $\lambda_2 > \lambda_{12}$ and $\lambda_4 > \lambda_{14}$.

Let, $$\Delta g = I_2\{(\lambda_2 + \lambda_4) - (\lambda_{12} + \lambda_{14})\} \tag{3.18}$$

or, $$G_{op} = \Delta g + \frac{g_{m16}}{2} \tag{3.19}$$

$$\text{Similarly, } G_{on} = \Delta g + \frac{g_{m15}}{2} \tag{3.20}$$

$$\text{And,} \quad A_v = \frac{g_{m2}}{G_{op}} = 2\frac{g_{m2}}{\left(2\Delta g + g_{m16}\right)} \tag{3.21}$$

Thus, bulk effects will decrease the small-signal gain, and it will also be slightly dependent on the channel length and technology.

3.4 Common-Mode Feedback (CMFB) Circuit

As seen from Figures 3.3 and 3.4, the differential-out gain stage needs a common-mode feedback (CMFB) circuit for the stabilization of the output common-mode voltage. This is needed because as the common-mode voltage at the differential inputs change, the output common-mode voltage will also tend to change largely causing some of the devices to depart from saturation to triode region of operation. The purpose of the CMFB circuit is to hold the common-mode voltage at the outputs close to a constant value so that all the devices operate in saturation. The negative resistance block, shown in Figure 3.4, not only generates the small-signal negative resistance, but it also acts as a CMFB circuit. If the common-mode voltage at the inputs changes, the common-mode voltage at the output nodes will tend to change accordingly. The CMFB circuit will oppose this change at the output common-mode voltage. In Figure 3.4, let us assume that due to the change in input common-mode voltage, the input and the output common-mode voltages change as

$$\Delta V_{ip} = \Delta V_{in} = \Delta V_i \text{ and } \Delta V_{op} = \Delta V_{on} = \Delta V_o \tag{3.22}$$

Neglecting the contribution from the "$1/g_m$" loads, the gain from V_{op} (gate of M_7) to V_{on} (gate of M_8) can be approximated as

$$A_{7,8} = -\frac{\left(g_{ds11} + g_{ds13}\right)}{\left(\frac{g_{ds7}g_{ds11}}{g_{m7}} + \frac{g_{ds9}g_{ds13}}{g_{m9}}\right)} \tag{3.23}$$

The expression of $A_{7,8}$ in Equation (3.23) can also be visualized as the "*loop gain*" (LG) of the negative feedback loop, which tries to suppress common-mode voltage changes at the outputs. The "*open-loop*" common-mode gain from the differential inputs to the outputs is

$$A_{cm} = -\frac{\left(g_{ds5}/2\right)}{\left(\frac{g_{ds1}g_{ds5}}{2g_{m1}} + \frac{g_{ds3}g_{ds6}}{2g_{m3}}\right)} \tag{3.24}$$

So, in presence of the common-mode negative feedback loop at the outputs, the change in output common-mode can be expressed as

$$\Delta V_o = \Delta V_i \left[\frac{A_{cm}}{1 - A_{7,8}}\right] \tag{3.25}$$

Comparing Equations (3.23) and (3.24) and using Table 4.1, we will get

$$A_{cm} \cong \left(\frac{A_{7,8}}{2}\right) \tag{3.26}$$

Thus, Equation (3.25) can be approximated as

$$\Delta V_o \cong -\left(\frac{\Delta V_i}{2}\right) \tag{3.27}$$

Equation (3.27) shows that any input common-mode voltage change will be almost scaled down by a factor of 2 at the output. Notice that when the voltages at

the output nodes swing differentially (for a differential input voltage), there is no such negative feedback at the outputs.

As explained earlier, the circuit shown in Figure 3.4 can achieve an almost constant gain. If it is desired to achieve even higher gain, the circuit concept shown in Figure 2.13, can be implemented by removing the "1/ g_m" load stages at the outputs. The CMOS implementation of this concept is shown in Figure 3.7.

3.5 Gain Stage with Negative Resistance and Maximum Gain

Shown below is the implementation of the concept shown in Figure 2.13 to achieve maximum gain using the negative resistance circuit.

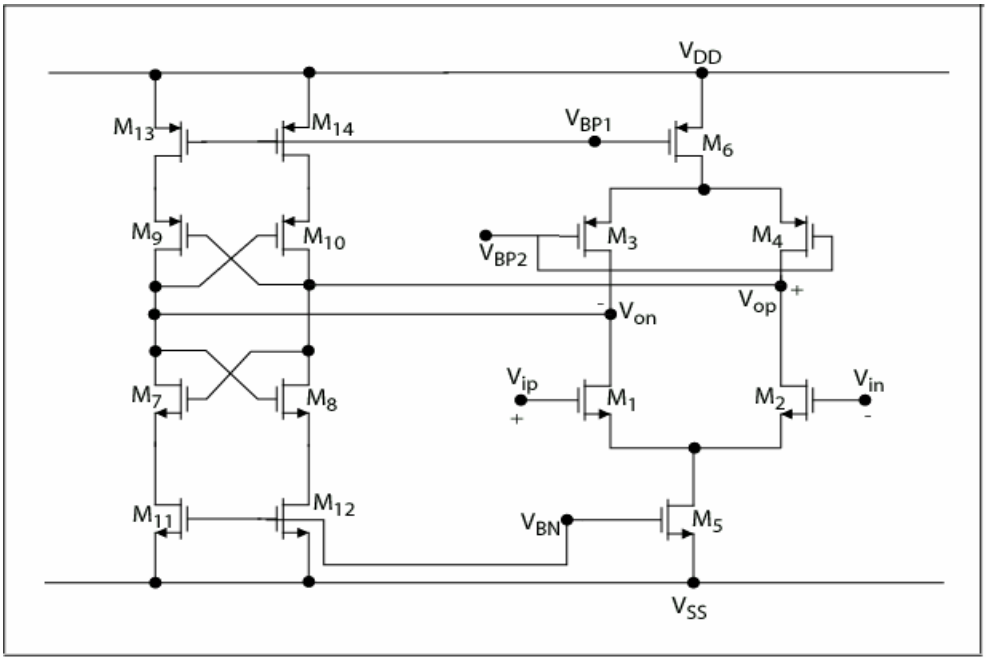


Figure 3.7. CMOS implementation of concepts of the gain stage with maximum gain

Table 3.2. Aspect ratios of the transistors of the gain stage with maximum gain

$S_1 = S_2 = (0.5)S_5 = S_7 = S_8 = S_{11} = S_{12}$	500X
$S_3 = S_4 = (0.5)S_6 = S_9 = S_{10} = S_{13} = S_{14}$	1000X

* $S_i = \left(\frac{W}{L}\right)_i$

The equivalent, small-signal conductance model for Figure 3.7 is shown next in Figure 3.8.

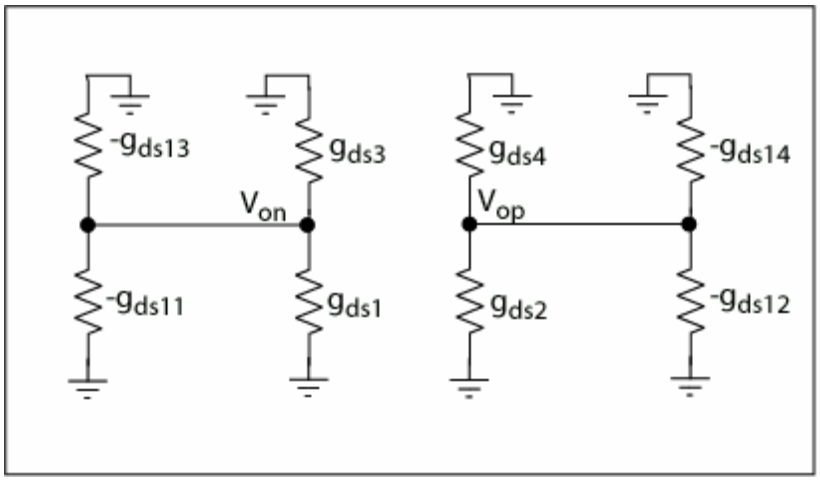


Figure 3.8 Small-signal conductance based model for the gain stage with maximum gain

The total conductance at the positive output can be given by

$$G_{op} = (g_{ds2} + g_{ds4}) - (g_{ds12} + g_{ds14}) \tag{3.28}$$

or, $$G_{op} = I_2(\lambda_2 + \lambda_4) - I_{12}(\lambda_{12} + \lambda_{14}) \tag{3.29}$$

Assuming normal input common-mode condition, $I_2 = I_{12}$, we will get

$$G_{op} = I_2\{(\lambda_2 + \lambda_4) - (\lambda_{12} + \lambda_{14})\} \tag{3.30}$$

As explained earlier, due to bulk effects, the total conductance is finite and positive, and Equation (3.30) can be modified as

$$G_{op} = \Delta g \tag{3.31}$$

where, $\Delta g = I_2\{(\lambda_2 + \lambda_4) - (\lambda_{12} + \lambda_{14})\}$.

So, the small-signal gain can be expressed as

$$A_v = \frac{g_{m2}}{\Delta g} \tag{3.32}$$

It can be seen that bulk effects tend to reduce A_v. As discussed previously, there is another limitation that decreases A_v, and it is caused due to the non-ideal MOS source followers (M_7 through M_{10}) in the negative resistance block of Figure 3.7. The voltage gain of these followers is less than unity ($A_f < 1$). Thus, Equation (3.28) can modified as

$$G_{op} = I_2(\lambda_2 + \lambda_4) - I_{12}A_f(\lambda_{12} + \lambda_{14}) \tag{3.33}$$

or, $$G_{op} = I_2\{(\lambda_2 + \lambda_4) - A_f(\lambda_{12} + \lambda_{14})\} \tag{3.34}$$

The value of G_{op} from Equation (3.34) will be greater than that from Equation (3.30) as the follower gain is less than unity. This will cause a further reduction in the value of A_v from its original value given by Equation (3.32).

In the next section, the biasing scheme for the gain stages is discussed. It uses an adaptive PMOS bulk drive mechanism to generate constant bias currents.

3.6 Bias Circuit

Two $L_{\min}$ based gain stages were developed in the previous sections, and they were shown in Figures 3.4 and 3.7. In both of these circuits, the bias voltages V_{BP1}, V_{BP2}, and V_{BN} need to be designed. This section focuses on the development of a suitable biasing stage to generate the biasing voltages and currents for the gain stages. The most commonly used way of generating bias currents is to generate a reference current using a bootstrap circuit [1], which is then mirrored onto different stages. When using $L_{\min}$ based devices, current mirrors deviate appreciably from their ideal behavior due to large channel length modulation effects. Small channel length devices have large channel length modulation parameter, λ. But, if the drain-to-source voltages (V_{DS}) of the mirroring and mirrored transistors can be matched, almost ideal current mirroring can be achieved even with smaller channel lengths. This principle of matching of the V_{DS} is used in this design.

Before designing the biasing stage, let us look at the quiescent voltages of the transistors (M_7 through M_{14}) in the negative resistance block of Figures 3.4 and 3.7. Considering the transistors M_7 through M_{10}, the quiescent biasing condition of these 4 transistors is

$$V_{GS} = V_{DS} \tag{3.35}$$

The transistors M_{11}, M_7, M_9, and M_{13} form a stack between the power supply rails. As discussed in Chapter 2, small channel lengths cause non-ideal current

mirroring where the mirrored current can vary largely from the reference current. The biasing of M_{11} and M_{13} should be such that proper mirroring can occur, which will be possible only by the matching of V_{DS} of the mirroring and the mirrored transistors. The proper mirroring of currents is important because while using the negative resistance generation circuit, mismatched currents may result in negative effective conductance at the output nodes, which is undesirable for proper circuit operation. To attain proper current mirroring, the biasing circuit of the two gain stages (referred to as BIAS stage) is shown in Figures 3.9 and 3.10, and the biasing scheme is described next.

In Figures 3.9 and 3.10, the BIAS stage consists of 4 diode-connected transistors (M_{23} through M_{26}). As stated earlier, the quiescent biasing condition for M_7 through M_{10} is

$$V_{GS} = V_{DS}$$

Now, based on the quiescent biasing conditions of M_7 through M_{10}, the only possible quiescent biasing condition for M_{11} through M_{14} is

$$V_{GS} = V_{DS}$$

Thus, by matching the drain-to-source biases, proper current mirroring can be attained with $L_{\min}$ devices. The gain stages with their biasing circuits are shown in Figures 3.9 and 3.10. A diode-connected stack of transistors is used to generate the reference biasing current, which is then mirrored on to the following stages.

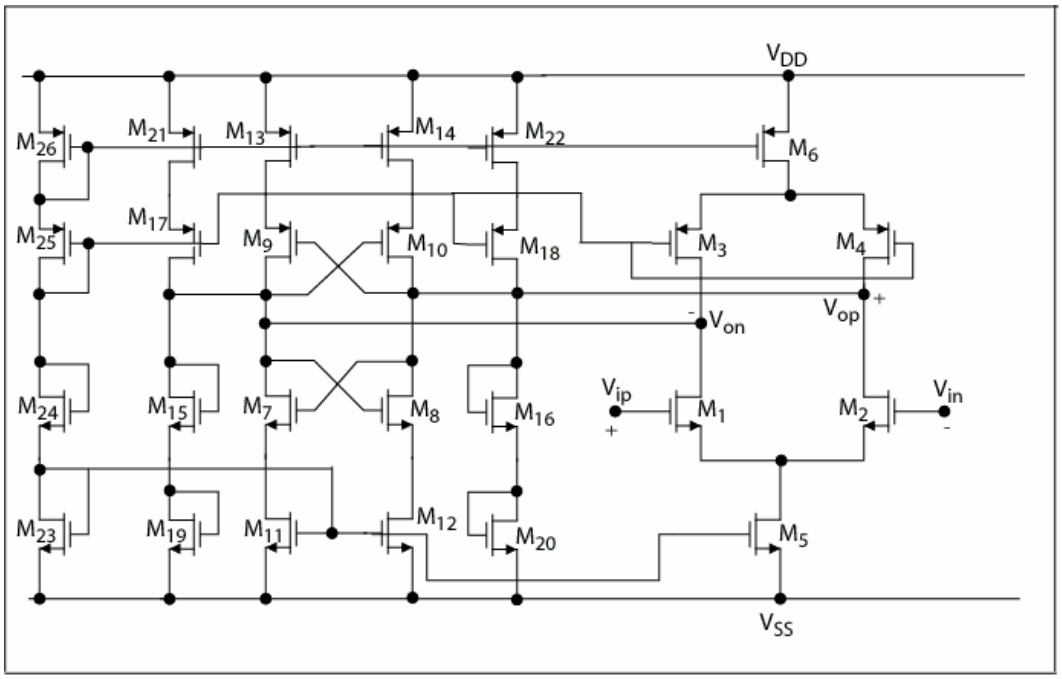


Figure 3.9. Gain stage for constant gain with its biasing stage

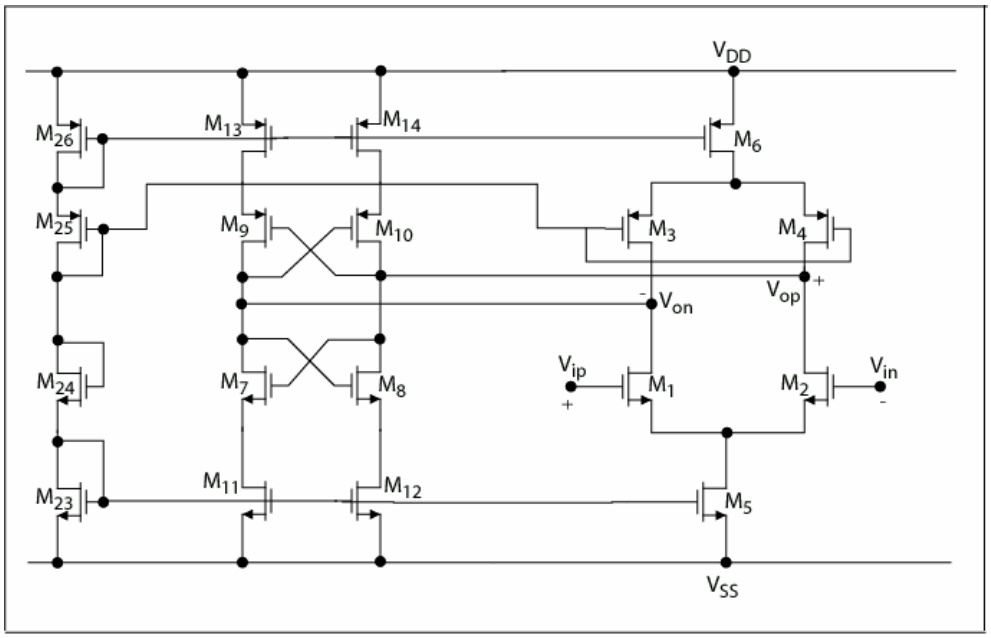


Figure 3.10. Gain stage for maximum gain with its biasing stage

In Figures 3.9 and 3.10, proper mirroring of the reference bias current will happen as the drain-to-source voltages of the mirroring and mirrored transistors are matched. Some concerns that might arise due to the use of the diode-connected transistor stack for biasing are:

1. Poor power supply rejection as any ripple in the supply rails can cause appreciable change in the bias current.
2. Variation in the bias current with technology and channel length.
3. Variation in the bias current with temperature.

Out of the above 3 points, it will be shown that the first 2 concerns can be overcome, and they are explained in the later sections.

3.7 Constant Bias Current Generation

One of the most widely used ways of generating the reference bias current is by using the Bootstrap circuit [1]. But, in the gain stages developed here, the reference bias current is generated in the diode-connected transistor stack. This reference current should be independent of the technology as well as the channel length. The overall reference current generation scheme is shown next in Figure 3.11.

In past, successful bulk drive schemes (named as "Current Driven Bulk" schemes) have been used to modulate the threshold voltage of the MOS devices [33, 34]. In this research, the biasing scheme uses an adaptive PMOS bulk-drive mechanism to generate a constant reference current. In this scheme, the bulks of

the PMOS transistors are driven, but the bulks of the NMOS transistors are always tied to the lowest circuit potential (V_{SS}) in order to avoid latch-up. Thus, the threshold voltage of the PMOS devices is modulated. The bias current generation circuit is shown next in Figure 3.11.

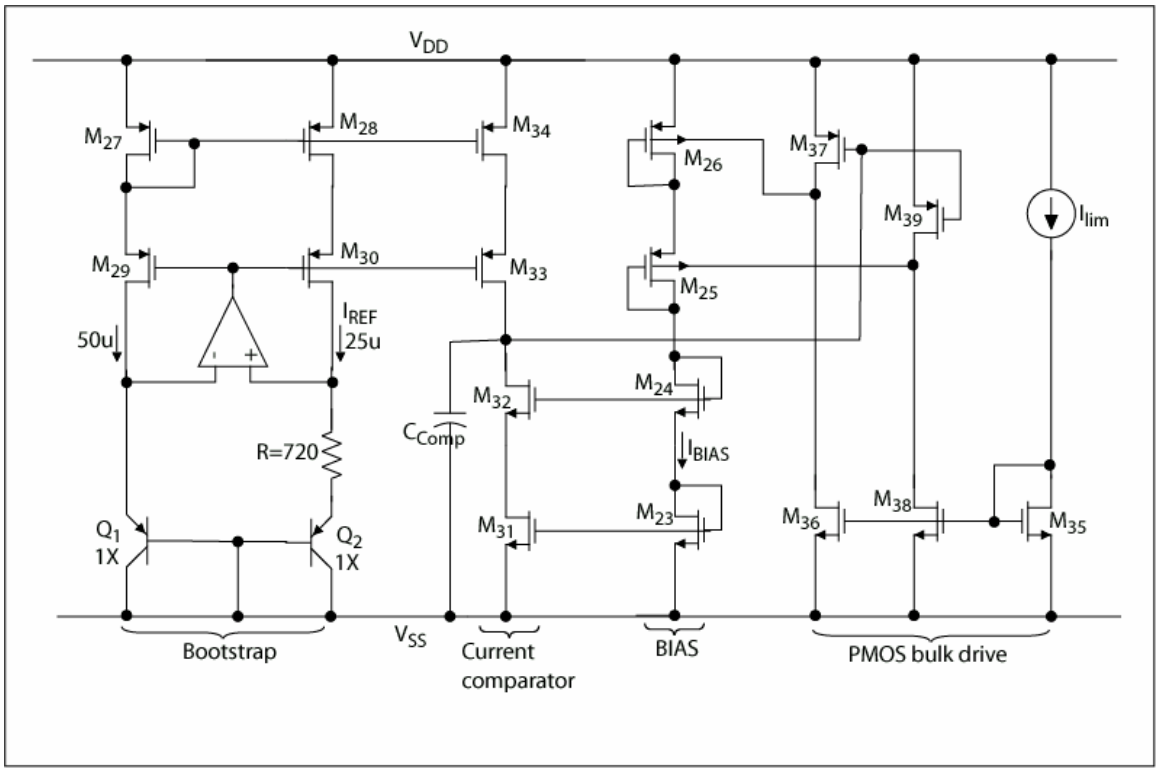


Figure 3.11. Bias current generation scheme

Table 3.3. Aspect ratios of the transistors in the bias current generation circuit

$S_{23} = S_{24} = S_{31} = S_{32}$	500X
$S_{25} = S_{26}$	1000X
$S_{28} = S_{30} = S_{33} = S_{34}$	200X
$S_{27} = S_{29}$	400X

* $S_i = \left(\frac{W}{L}\right)_i$

In Figure 3.11, the diode-connected transistors M_{23} through M_{26} constitute the "BIAS" block as shown in Figures 3.9 and 3.10. The "Bootstrap" block is used to generate a constant current across different technologies and channel lengths. This stage is similar to a "Bandgap stage", and the reference current is proportional to absolute temperature. The bipolar p-n-p devices are implemented using substrate p-n-p transistors. The collector, which is the p-substrate, should always be tied to the lowest potential in the circuit. The op amp, shown in the Bootstrap block, was used to equate the voltages at the drains of M_{29} and M_{30}. This op amp was implemented using a two-stage op amp with current mirror load. It is important to keep the offset voltage of this op amp as small as possible in order to generate a constant reference current. The value of the reference current in the "Bootstrap" block was set at $25\,\mu A$.

The "Current comparator" block compares the two currents in the "Bootstrap" and the "BIAS" blocks. The "PMOS bulk-drive" block drives the

bulks of the PMOS transistors of the "BIAS" block. The current source $I_{\lim}$ can be implemented using another Bootstrap circuit, and this current sets the maximum limit of the forward-biased PMOS bulk drive current. In this design, this limit was set to 250 nA. In Figure 3.11, the bulk drive of only the PMOS transistors (M_{25} and M_{26}) are shown. Although it is not shown in Figures 3.9 and 3.10, the bulks of all the PMOS transistors are also driven in these figures. For reasons of simplicity, only the bulk drives of the PMOS transistors (M_{25} and M_{26}) are shown in Figure 3.11, but it is not shown in Figures 3.9 and 3.10. Bulk drive helps in keeping the threshold voltage constant for all the PMOS transistors, and it ensures good current mirroring of the biasing currents. The aspect ratios for M_{35} through M_{39} can be chosen at will such that they can carry the limiting current $I_{\lim}$.

Let us understand the working of the bias current generation circuit shown in Figure 3.11. This circuit is designed with the aim of generating a constant bias current (I_{BIAS}) in the "BIAS" stage across different technologies and channel lengths. The desired reference current is generated in the "Bootstrap" block. This reference current is relatively independent of the power supply as well as the technology. But, it is dependent on temperature. The reference current in this design was fixed at 25 μA. It can be conveniently chosen to a desired value by changing the resistance in the "Bootstrap" circuit. The "Current comparator" block compares this reference current with the current I_{BIAS} in the "BIAS" stage. Since the reference current will remain relatively constant independent of the

power supply and the technology; it is desired that the current I_{BIAS} should also remain constant. The "Current comparator" and the "PMOS bulk drive" blocks, together form a negative feedback loop, which tends to keep I_{BIAS} constant.

Let us assume that I_{BIAS} is less than the reference current (25 μA). The current comparator will compare the two currents: the reference current and I_{BIAS}, and its output (drains of M_{32} and M_{33}) will go high. In the "PMOS bulk drive" block, the transistor pairs (M_{36}, M_{37}) and (M_{38}, M_{39}) form two inverter stages. As the output of the "Current comparator" block goes high, the output of these two inverters will go low, which in turn will forward bias the bulks of the PMOS transistors (M_{25} and M_{26}). This will decrease the threshold voltages of the PMOS transistors, thus increasing the current I_{BIAS} flowing through them. There is a maximum limit to the forward biasing of the PMOS bulks, and it is set by the limiting current $I_{\lim}$ in the "PMOS bulk drive" block. This limiting current sets the maximum value of the forward biased PMOS bulk current. Thus, there is a minimum limit to which the threshold voltage of the PMOS transistors can be decreased, which in turn puts a limit on the value of I_{BIAS}. So, across different technologies and channel lengths, there is a possibility that even with the efforts of the current comparator and bulk drive, the value of I_{BIAS} might remain less than the reference current.

On the other hand, if the value of I_{BIAS} is greater than the reference current, the outputs of the current comparator and the subsequent inverters will go low and high respectively. This will tend to increase the reverse bias on the

PMOS bulks, thus increasing their threshold voltages, which in turn will cause a decrease in I_{BIAS}. The limiting condition here is when the output of the inverters approach V_{DD}. This becomes the maximum limit of the reversed-biased voltage at the PMOS bulks, thus setting a minimum limit on I_{BIAS}. So, it is possible that across different technologies and channel lengths, the value of I_{BIAS} might remain larger than the reference current.

The same arguments presented above can be used to explain a relatively constant value of I_{BIAS} with power supply variations. If the power supplies vary, forward and reverse biasing of the PMOS bulks will tend to keep I_{BIAS} close to the reference current. The compensation of the negative feedback loop comprising of the "Current comparator", "BIAS", and "PMOS bulk drive" blocks is important. In general, it can be compensated by the capacitor C_{comp} attached to the output of the current comparator, which is a high impedance node, and it will create the dominant pole. In this design, the parasitic capacitance at the cascoded output was large enough to compensate the loop.

When forward biasing the PMOS bulks, one obvious concern is the operation of the parasitic substrate bipolar p-n-p (p^+ source - n well – p substrate) transistor. If the current gain β of this transistor is appreciable, it will cause large drain of current through the p^+ source diffusions as the emitter current. If the depth of the n well (base width) is large enough, it will result in very small value of the current gain β, which will make the collector current flowing out of the p substrate negligible. Thus, the emitter current will be equal to

the base current, i.e., the forward-biased diode current flowing out of the p^+ source will be equal to the current in the n well.

The bias current generation circuit shown in Figure 3.11 will be used to generate the bias currents for a two-stage op amp, which will be discussed in the following chapters. The circuit of Figure 3.11 can also be used to generate a bias current, which is a multiple of the reference current in the "Bootstrap" block. The reference current in Figure 3.11 was 25 μA, and referring to Table 3.3 for the aspect ratios, the value of the bias current I_{BIAS} should also be 25 μA because the aspect ratios of M_{23}, M_{24}, M_{31}, and M_{32} are equal. Using the same circuit, a different bias current, which is a multiple (k) of the reference current, can be generated. If the aspect ratios of M_{23} and M_{24} is k times the aspect ratios of M_{31} and M_{32}, the current comparator will compare the reference current to I_{BIAS}/k, and the value of I_{BIAS} will be k times the reference current (25 μA). These large values of I_{BIAS} will be possible through forward biasing of the bulks of the PMOS transistors, but within the limits of the forward biased bulk current.

A sample simulation of the bias current generation scheme in a 0.25 μm CMOS technology is shown next in Figure 3.12. The magnitude of the reference current in the Bootstrap circuit was 25 μA, and the current comparator tried to make the value of I_{BIAS} equal to 25 μA in the presence of power supply variations. The aspect ratios of the transistors are shown in Table 3.3.

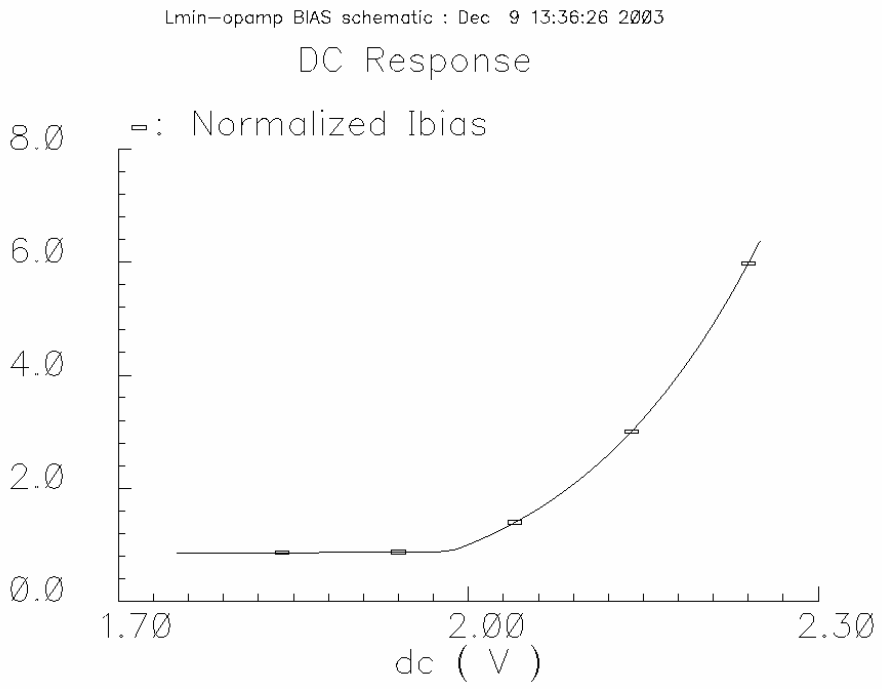


Figure 3.12. Variation of normalized I_{BIAS} with V_{DD}

The normalized variation of I_{BIAS} with V_{DD} is shown in Figure 3.12. The bias current was normalized with respect to its nominal value of 25 μA. As the value of the supply voltage V_{DD} is decreased, the bulks of the PMOS transistors are forward biased to keep I_{BIAS} constant. The bias current does not remain exactly constant and its normalized variation in the lower supply voltage ranges is enlarged and shown next in Figure 3.13.

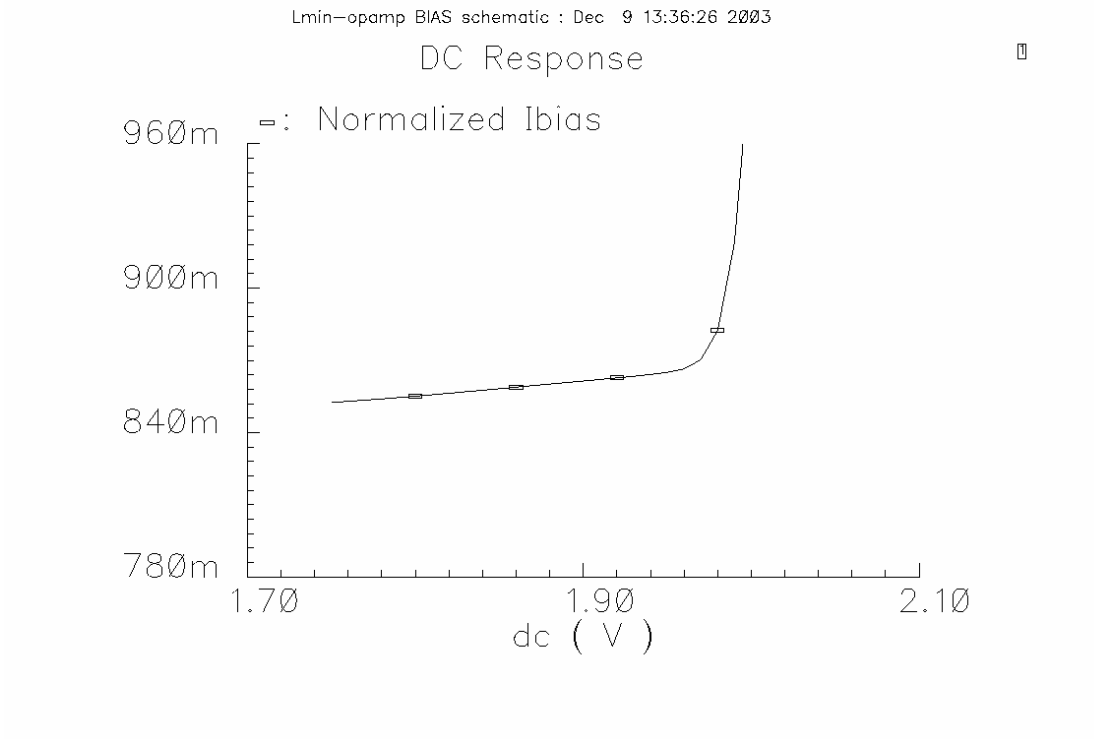


Figure 3.13. Variation of normalized I_{BIAS} with V_{DD} for lower values of V_{DD}

In absence of any bulk drive, with decreasing V_{DD}, the bias current will have decreased exponentially as the devices operate in weak inversion. But, due to the adaptive PMOS bulk drive scheme, the bias current does decrease slightly, but the variation is linear and much smaller than an exponential decrease in the current.

On the other hand, when V_{DD} increases, the bulks of the PMOS devices are reversed biased in order to keep I_{BIAS} constant. But, the maximum limit of the reversed biased voltage at the bulks is limited by V_{DD} itself. Thus, for increasing supply voltages, the threshold voltage of the PMOS devices gets saturated at a maximum value, and the current increase exponentially. The plot of

the natural logarithm of normalized I_{BIAS} with V_{DD} is shown next in Figure 3.14.

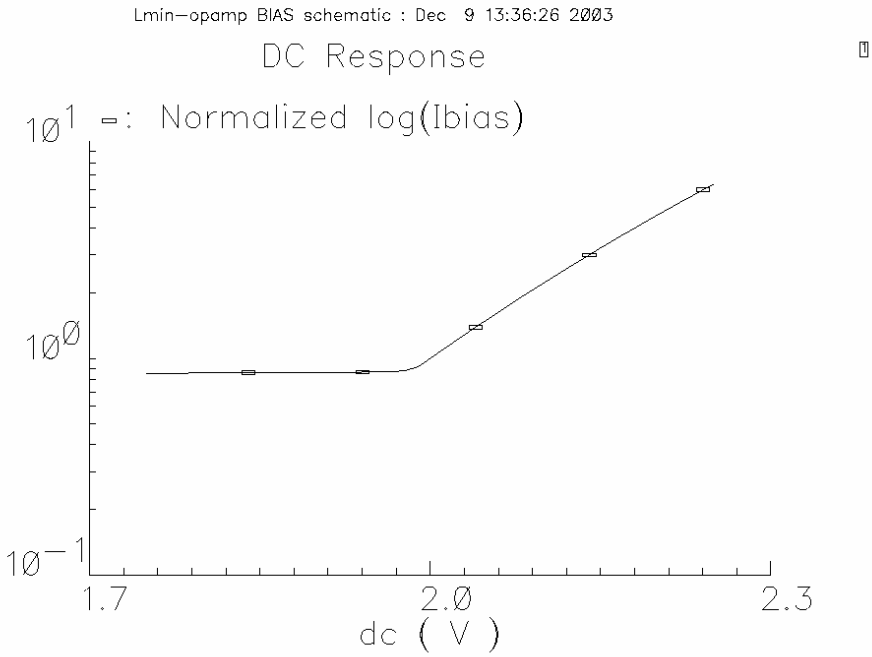


Figure 3.14. Plot of normalized $\{\ln(I_{BIAS})\}$ with V_{DD}

For higher supply voltages (V_{DD} > 2 V), the bias current changes exponentially, and it can be seen as an almost straight line in Figure 3.14. As the supply voltage further increases, the gate-to-source voltages, V_{GS}, of the transistors increase causing them to operate in stronger inversion from weak inversion. This can be seen in Figure 3.14 where the slope of the line decreases for large supply voltages showing a gradual change from the exponential to square law behavior of the device.

3.8 Summary

The transistor level implementation of two $L_{\min}$-based gain stages were discussed in this chapter. Using a negative resistance circuit, the small-signal gain can be increased while using all minimum channel length devices. The negative resistance circuit also acts at the CMFB circuit for the differential output gain stage. Bulk effects and non-ideal MOS source followers tend to generate finite positive conductances at the outputs, and they degrade the small-signal voltage gain.

The biasing scheme for the two $L_{\min}$-based gain stages was also discussed in this chapter. The bias current was generated using a diode-connected stack of transistors, and it was kept relatively constant using an adaptive PMOS bulk drive scheme. The threshold voltages of the PMOS devices were modulated by bulk drive, and suitable bias currents were generated and mirrored into the blocks of the gain stages. Simulation results for this biasing scheme are presented, and the measurement results will be presented in the next chapter.

In the next chapter, the design of the overall, two-stage op amp will be presented. The op amp has two cascaded gain stages, where each of the gain stage has identical devices as discussed in the previous chapter. The op amp is compensated using two Miller compensation capacitors for a constant phase margin, which is made relatively insensitive to the channel length and the technology.

Chapter 4

Two-stage, Miller-Compensated Op Amp with Constant Phase Margin

In the previous chapter, the design of two $L_{\min}$-based gain stages were discussed along with their biasing schemes. The first gain stage (as shown in Figure 3.9) was designed to achieve constant small-signal gain across different technologies while using all minimum feature-size channel length devices. In this chapter, this gain stage is used to develop a two-stage op amp (referred to as *OP*1). This op amp was simulated in a 0.25 μm CMOS and a 0.18 μm CMOS technology with all minimum feature-size channel length devices in each of them, and the results are presented in this chapter. This op amp was not fabricated and only the simulation results are presented.

The second gain stage (as shown in Figure 3.10) was designed to achieve the maximum possible gain for a given bias current. This gain stage is used to develop a two-stage op amp (referred to as *OP*2). This op amp was fabricated in both the CMOS technologies, and their simulation and measurement results are presented in this chapter.

In both the op amps, even though all the performance specifications cannot be kept constant, both of these op amps are designed to achieve a constant phase margin across different technologies. Both of them have the same compensation scheme, and they are compensated using two Miller feedback capacitors. The phase margin is expressed as the ratio of the biasing currents in the two gain stages, which can be kept constant across different technologies.

4.1 Op Amp Compensation

The two-stage op amp consists of two gain stages as shown in Figure 4.1. The gain stages are shown in the figure as G_1 and G_2. Both of these gain stages are identical, i.e., they have the same aspect ratio of the transistors in both the gain stages, and they have the same architecture as shown in Figure 3.9. The op amp is compensated using a simple Miller compensation scheme [1], and it is described next. The choice of this simple compensation scheme was made because this scheme can be used to maintain a constant phase margin across different technologies with the same component parameters (capacitors).

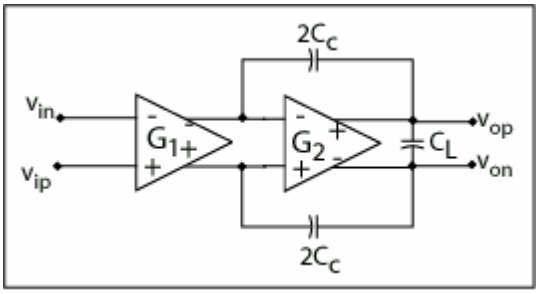


Figure 4.1. Two-stage op amp with Miller compensation

Since the op amp is designed with the aim to develop a technology and channel length independent architecture, the compensation of the op amp should be insensitive to the technology as well as the channel length. As it will be shown later, the phase margin of this op amp can be expressed as a ratio of transconductances, which will make it insensitive to the technology and the channel length. Even though the proposed scheme will ensure a constant phase

margin, the unity gain-bandwidth frequency (UGBW) will depend on both the technology and the channel length. The following section describes the compensation of the op amp in Figure 4.1.

Let, g_{m1} = transconductance of the first gain stage (G_1).

R_1 = load impedance to ac ground seen at each of the output nodes of G_1.

g_{m2} = transconductance of the second gain stage (G_2).

R_2 = load impedance to ac ground seen at each of the output nodes of G_2.

$C_{L,\max}$ = maximum external differential load capacitance to be driven.

A_{V1}, A_{V2} = gains of G_1 and G_2 respectively.

We have

$$A_{V1} = g_{m1}R_1 \quad \text{and} \quad A_{V2} = g_{m2}R_2 \tag{4.1}$$

In the following analysis, it is assumed that the op amp is operated in the single-ended output configuration, and the other output node is left floating. Thus, the overall gain for the single-ended output configuration is given by

$$A_V = A_{V1}\frac{A_{V2}}{2} \tag{4.2}$$

The dominant pole (at the outputs of G_1) is given by

$$p_1 = \frac{-1}{R_1(A_{V2})(2C_C)} \tag{4.3}$$

The load pole (at the outputs of G_2) can be given by

$$p_L = \frac{-g_{m2}}{(2C_{L,\max})} \tag{4.4}$$

The UGBW frequency, while operating the op amp in single-ended output configuration, is given by

$$UGBW = A_V p_1 = \frac{g_{m1}}{4C_C} \tag{4.5}$$

The smallest pole to occur is the dominant pole (p_1), followed by the load pole (p_L) caused by the external capacitor. If the UGBW is smaller than the load pole, the system can be made stable. The ratio of the UGBW to the load pole is given by

$$\frac{UGBW}{p_L} = \left(\frac{g_{m1}}{g_{m2}}\right)\left(\frac{C_{L,\max}}{2C_C}\right) \tag{4.6}$$

Let us choose the value of the internal miller compensation capacitor to be

$$C_C = C_{L,\max} \text{ and let us choose, } g_{m2} = kg_{m1} \tag{4.7}$$

Then,
$$\frac{UGBW}{p_L} = \frac{1}{2k} \tag{4.8}$$

The right-half plane zero caused by the compensation capacitor is given by

$$z_{RHP} = \frac{g_{m2}}{2C_C} = -p_L \tag{4.9}$$

or,
$$\frac{UGBW}{z_{RHP}} = \frac{1}{2k} \tag{4.10}$$

If the scaling term k is set to 5, then Equations (4.8) and (4.10) will result in an approximate phase margin of 78.6 degrees. In the overall two-stage op amp shown in Figure 4.1, it can be seen that there are only two poles, which are given by Equations (4.3) and (4.4). There are no other higher order poles. But, there is a RHP zero caused by the gate-to-drain overlap capacitance of the differential input transistors of the first gain stage. Considering the current CMOS technologies, this higher order zero can be considered to be large.

Since the transistors are operated in weak inversion, the condition, $g_{m2} = kg_{m1}$ in Equation (4.7), can be achieved by scaling the bias current in G_2 by the factor k over the bias current in G_1. As stated earlier, the aspect ratios of the transistor in the two gain stages are identical. The scaling of the bias current in G_2 over G_1 can be achieved by the technique explained in Chapter 3. Referring to Figure 3.11, the scaling down of the aspect ratios of M_{31} and M_{32} over the aspect ratios of M_{23} and M_{24} will scale the bias current in the second gain stage.

When using smaller channel lengths, the ratio representing the phase margin will remain fixed even though the absolute value of bias currents and transconductances might change. Even though the UGBW frequency will vary, such a design will always be stable across different technologies and channel lengths. Higher stability with better phase margin can be achieved by increasing the scaling term k ($g_{m2} >> g_{m1}$). In the following sections, other performance specifications of the op amp are discussed.

4.2 Slew Rate

Referring to Figure 4.1, the slew rate of the op amp can be given by

$$SR = \min\left[\left(\frac{I_{BIAS1}}{2C_c}\right),\left(\frac{I_L}{2C_L}\right)\right] \tag{4.11}$$

where, I_{BIAS1} is the bias current in the first gain stage G_1, and I_L is the load current sourced or sunk into the single-ended output load capacitor. In general, when the output load capacitor is not very large, the slew rate can be approximated as

$$SR \cong \left(\frac{I_{BIAS1}}{2C_c}\right) \tag{4.12}$$

In most cases, the large-signal slewing of the op amp will depend on the compensation capacitor and the bias current in the first gain stage.

4.3 Input Referred Noise

Input referred noise of the op amp is an important performance specification for high-precision analog circuits. In CMOS op amps, there are mainly two major types of noises: (a) Flicker noise and (b) Thermal noise. In high-frequency op amps, the total noise is dominated by the thermal noise. Noise expressions and calculations can be found in [1]. The flicker noise at the input of the op amp is a low frequency noise, which can be viewed as similar to the dc input offset voltage. In switched-capacitors circuits, the dc offset and the flicker noise can be cancelled using the scheme shown in [35]. Further references to noise modeling and calculations can be found in [36]-[38].

In this research, the gain stage has been designed to achieve large small-signal gain. In Figure 4.1, most of the noise referred at the input will be due to devices in the first gain stage G_1. The gain stage, shown in Figure 3.10, is drawn again in Figure 4.2 for the purpose of noise calculations. It can be seen that since this gain stage has almost twice the number of devices as compared to a conventional differential gain stage, its input referred noise will be larger than the conventional gain stage.

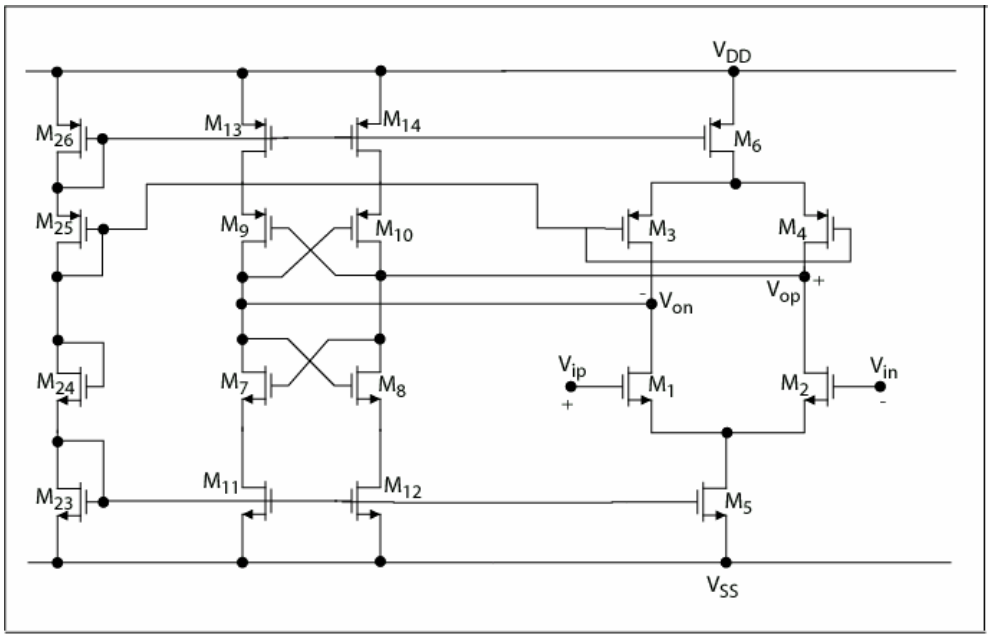


Figure 4.2. Gain stage of the op amp

In Figure 4.2, under differential operation, the sources of M_5 and M_6 remain at ac ground. Let us assume that the small-signal output resistance at each

of the two output nodes to ac ground is R_{out}. Due to the choice of the aspect ratios and the bias currents in the design, the transconductance of the PMOS devices are equal. The same is true for the NMOS devices too. For simplicity, let us represent the transconductance of the PMOS and NMOS devices by g_{mp} and g_{mn} respectively. In Figure 4.2, considering the differential output nodes and neglecting the noise contribution from the biasing circuit, the major contributors of noise at the outputs are M_1 through M_4 and M_{11} through M_{14}. The mean square noise voltage at the output can be calculated by summing all the mean square noise currents and multiplying it by the square of the output resistance. The total output referred mean square noise voltage at the differential outputs can be given by

$$e_{no}^2 = \left[2g_{m1}^2 e_{ni1}^2 + 2g_{m11}^2 e_{ni11}^2 + 2g_{m3}^2 e_{ni3}^2 + 2g_{m13}^2 e_{ni13}^2\right] R_{out}^2 \quad V^2/Hz \qquad (4.13)$$

where, e_{nij} corresponds to the mean-squared input referred noise voltage of the "j^{th}" transistor.

Due to the choice of equal aspect ratios and bias currents, we can write

$$e_{ni1}^2 = e_{ni11}^2 \text{ and } e_{ni3}^2 = e_{ni13}^2 \qquad (4.14)$$

Thus, we can modify equation (4.13) as

$$e_{no}^2 = 4\left[g_{m1}^2 e_{ni1}^2 + g_{m3}^2 e_{ni3}^2\right] R_{out}^2 \quad V^2/Hz \qquad (4.15)$$

The input referred noise voltage can be represented in terms of the output noise and the gain as

$$e_{ni}^2 = \frac{e_{no}^2}{g_{m1}^2 R_{out}^2} = 4\left[e_{ni1}^2 + \left(\frac{g_{m3}}{g_{m1}}\right)^2 e_{ni3}^2\right] \quad V^2/Hz \qquad (4.16)$$

Normally, the op amp will be operated in a closed loop with negative feedback, where its frequency response will be similar to a single-pole system. The worst-case feedback is the one where the feedback factor is unity. With negative feedback, the noise is present at the output till the UGBW frequency, beyond which the noise gets attenuated. Assuming that the frequency response of the overall op amp, operated in closed-loop with negative feedback, is similar to a single-pole frequency roll off, the product of the closed loop gain and the bandwidth is given by the UGBW frequency. Thus, using Equation (4.16) and assuming a single-pole system, the input referred noise voltage can be given by

$$e_{ni} \cong \sqrt{2\pi\left[e_{ni1}^2 + \left(\frac{g_{m3}}{g_{m1}}\right)^2 e_{ni3}^2\right] UGBW} \qquad \text{V} \qquad (4.17)$$

Equation (4.17) gives an estimate of the noise voltage at the input of the op amp irrespective of the feedback factor. The output noise can be calculated by multiplying the input noise voltage by the closed-loop system gain. Since, the op amp in closed loop is not a single-pole system, the actual input referred noise voltage will be less than the noise voltage given by Equation (4.17).

The input referred noise voltage, given by Equation (4.17), is a generalized expression. At low frequencies, the flicker noise will be dominant. As explained earlier in Chapter 2, when using small channel length devices, the flicker noise can be reduced by using large device widths. In this design, the use of large widths help in achieving reduced flicker noise. At higher frequencies, the thermal noise is dominant. The thermal noise voltage is inversely proportional to the transconductance, and it can be reduced by larger biasing currents.

4.4 Input Common-Mode Range (ICMR)

The input common-mode range (ICMR) of an op amp is one of its important specifications. The op amp designed here does not qualify as a rail-to-rail op amp (whose inputs can swing all the way to the power supply rails). The ICMR of this op amp is limited by the threshold voltages of the devices, and it is explained next.

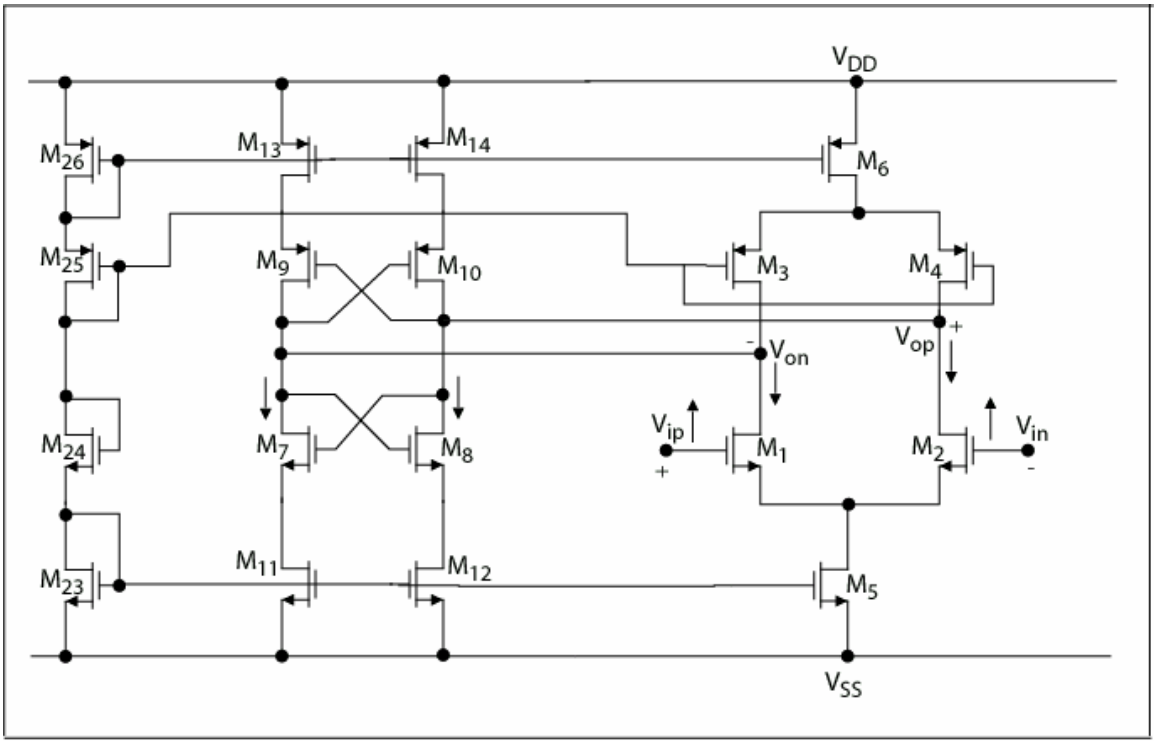


Figure 4.3. Effect of the variation of input common-mode voltage in a single gain stage

The value of the minimum input common-mode voltage can be expressed as

$$V_{IC}(\min) = V_{SS} + V_{T1} + V_{ds1}(sat) + V_{ds5}(sat) \tag{4.18}$$

Since the transistors are operated in weak inversion, V_{gs} is smaller than V_T, and it can be assumed that

$$V_{ds1}(sat) = V_{ds5}(sat) \cong 0.1 \text{ V} \tag{4.19}$$

Thus, $$V_{IC}(\min) \le V_{SS} + V_{T1} + 0.2 \text{ V} \tag{4.20}$$

The calculation of the maximum input common-mode range is described next. For sake of simplicity, let us assume that the negative resistance block in Figure 4.3, which also acts as the CMFB circuit, holds the common-mode voltage at the output nodes as

$$V_{ocm} = V_{DD} - \left\{ \left| V_{T10} \right| + \left| V_{T14} \right| + V_{ds10}(sat) + V_{ds14}(sat) \right\} \tag{4.21}$$

or, $$V_{ocm} = V_{DD} - \left\{ \left| V_{T10} \right| + \left| V_{T14} \right| + 0.2 \right\} \tag{4.22}$$

Now, the maximum input common-mode voltage can be given by

$$V_{IC}(\max) = V_{ocm} + V_{T1} \tag{4.23}$$

As V_{gs} of the transistors is smaller than V_T

$$V_{IC}(\max) \ge V_{DD} + V_{T1} - \left\{ \left| V_{T10} \right| + \left| V_{T14} \right| + 0.2 \right\} \tag{4.24}$$

Equations (4.20) and (4.24) give the minimum and maximum value of the ICMR. It can be seen the maximum and minimum input common-modes voltages are less than the power supply rails by approximately a threshold voltage of the PMOS and the NMOS devices respectively.

When the input common-mode voltage changes, the distribution of the currents in the differential gain stage and the negative resistance stage are not identical. Figure 4.3 shows a single gain stage of the op amp. It is important to

study the output resistance for large signal conditions, which will cause mismatches in the drain currents. The directions of the arrows in this figure correspond to the movement (increase or decrease) of the voltages at those nodes. In this figure, the common-mode voltage at both the inputs is shown to increase equally by the arrows. This causes the output common-mode voltages to decrease. The corresponding changes in the bias currents in the transistors are tabulated next.

Table 4.1. Change in the bias currents of different transistors with an increase in the input common-mode voltage

Transistors	Change in the bias currents from its nominal value
M_1, M_2, M_3, and M_4	Increases
M_7, M_8, M_9, and M_{10}	Decreases

Table 4.2. Change in the bias currents of different transistors with a decrease in the input common-mode voltage

Transistors	Change in the bias currents from its nominal value
M_1, M_2, M_3, and M_4	Decreases
M_7, M_8, M_9, and M_{10}	Increases

From Table 4.1, it can be seen that as the input common-mode voltage increases, the effective conductance at the output becomes positive. This happens because the current in the differential gain stage increases causing an increase in the positive output conductance, but the current in the negative resistance block decreases causing a decrease in the negative output conductance. Thus, the effective output conductance becomes positive, and this causes the small-signal gain to decrease with increase in the input common-mode voltage.

It can also be seen from Table 4.2 that for a decrease in the input common-mode voltage, using the same arguments as above, it can result in a negative effective output conductance and a finite small-signal gain. In practice, most of the op amps are operated in closed-loop configurations employing negative feedback. In presence of an external negative feedback, it will try to make the effective output conductance positive.

4.5 Power Supply Rejection Ratio (PSRR)

One obvious concern while using the diode-connected stack of the devices in the bias circuit (in Figure 3.11) is its sensitivity to the power supply variations. As it has been explained in the previous chapter, through an adaptive forward and reversed biasing of the PMOS bulks, a power supply independent bias current can be generated in the diode-connected stack of the biasing circuit. In this section, a small-signal analysis under power supply variation is described.

Referring to Figure 4.3, the widths of the PMOS transistors are kept twice as that of the NMOS transistors because for the same bias current, it will result in approximately the same value for the transconductance for both of types of devices. For simplicity, the body effect will be neglected for PSRR calculations. The transconductances for the PMOS and NMOS transistors are represented as g_{mp} and g_{mn} respectively, and they are assumed to be approximately equal in the following analysis.

In Figure 4.3, let, v_S be a small ripple in the positive power supply rail. The ripple at the gate of M_6, which propagates through the BIAS circuit, can be approximately given by

$$v_{g,M6} = \left(\frac{\left(g_{mp} + 2g_{mn}\right)}{2\left(g_{mp} + g_{mn}\right)} \right) v_S \tag{4.25}$$

The ripple at the gate of M_5 can be approximately given by

$$v_{g,M5} = \left(\frac{g_{mn}}{2\left(g_{mp} + g_{mn}\right)} \right) v_S \tag{4.26}$$

The small-signal current in M_6 will be

$$i_{M6} = \left(\frac{{g_{mp}}^2}{2\left(g_{mp} + g_{mn}\right)} \right) v_S \tag{4.27}$$

The small-signal current in M_5 will be

$$i_{M5} = \left(\frac{{g_{mn}}^2}{2\left(g_{mp} + g_{mn}\right)} \right) v_S \tag{4.28}$$

The differential output current i_{out} can be given by

$$i_{out} = \pm(i_{M6} - i_{M5}) = \pm\left(\frac{(g_{mp} - g_{mn})}{2}\right)v_S \tag{4.29}$$

If the transconductance of the PMOS and the NMOS transistors can be made approximately equal, then the effect of a power supply ripple at the output will be negligible, and it will result in high PSRR.

In the next sections, the simulation and measurement results for the two $L_{\min}$ based op amps, *OP*1 and *OP*2, are presented.

4.6 Simulation Results

Two $L_{\min}$-based op amp architectures were discussed in the previous sections. The gain stages used in these op amps were shown in Figures 3.9 and 3.10. As it was mentioned earlier, the gain stage shown in Figure 3.9 was designed to achieve an approximately constant small-signal gain with technology and channel length independence. The gain stage shown in Figure 3.10 was designed to achieve the maximum possible value of the small-signal gain.

The op amp, *OP*2, constituting the gain stage of Figure 3.10 was used to fabricate a two-stage op amp with all minimum feature-size channel length devices, whose simulation and experimental results are presented in the following sections. It was fabricated in a 0.25 μm CMOS process and a 0.18 μm CMOS

process to verify technology-independent phase margin, with minimum feature-size lengths in each of them. For the op amp, *OP*1, which was built using the gain stage of Figure 3.9 with all minimum feature-size channel length devices, only the simulation results are presented, as it was not fabricated.

Matching of the devices is an important issue while using minimum feature-size devices. In the following sections, along with the discussion of the overall op amp performance, measurements results for matching between the MOS transistors while using the minimum feature size channel length are also presented. And, some data relevant to the biasing circuit designed in Figure 3.11 are also presented.

4.6.1 Simulation Results of Op Amp *OP*1

In this section, the simulation results for the op amp, *OP*1, using BSIM3v3 models are presented. As mentioned earlier, this op amp architecture was not fabricated. It is a two-stage op amp (as shown in Figure 4.1) where each of the two gain stages is as shown next in Figure 4.4.

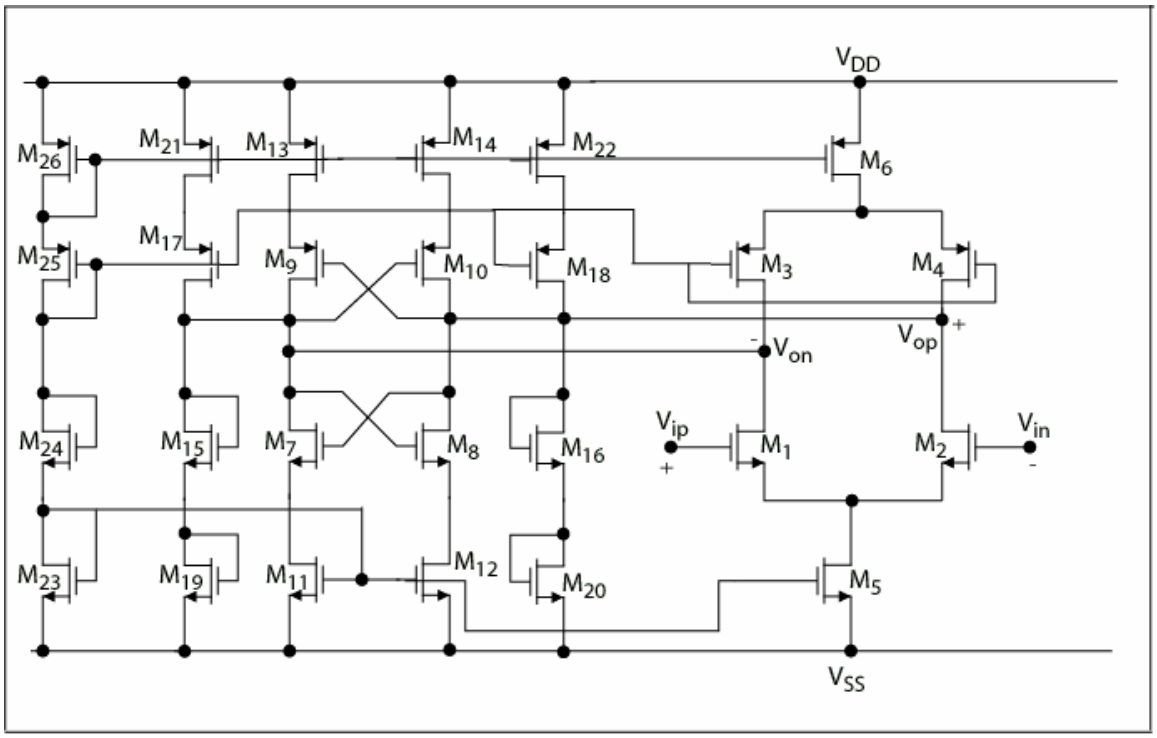


Figure 4.4. Gain stage of *OP*1

The gain stage, shown in Figure 4.4, tends to achieve an approximately constant small-signal gain across different technologies and channel lengths. The channel length of all the devices is the minimum feature-size length. The same architecture was simulated in a 0.25 μm CMOS process and a 0.18 μm CMOS process with minimum feature-size channel lengths in each of them, and the simulation results are presented next.

4.6.2 Simulation Results of *OP*1 in the 0.25 μm CMOS Process

The simulated performance of *OP*1 in the 0.25 μm CMOS process with all 0.25 μm channel length devices is summarized in Table 4.3. In the simulation setup, the op amp was connected in a single-ended output, unity gain buffer configuration.

Table 4.3. Simulated performance of *OP*1 in the 0.25 μm CMOS process

Performance specification	**Simulated value**
A_v	69 dB
UGBW (single-ended CL= 2 pF)	24 MHz
Phase margin	60 deg
Slew rate (single-ended CL= 2 pF)	+16, -12 $V / \mu s$
ICMR (Vdd = 2 V)	0.468 – 1.424 V
CMRR (at dc)	73 dB
PSRR (at dc)	72 dB
Input referred noise	6.28 $\mu V / \sqrt{Hz}$ (1 Hz) 0.6 $\mu V / \sqrt{Hz}$ (100 Hz) 14.7 $nV / \sqrt{Hz}$ (400 KHz: corner frequency)
Idd	817 μA

The simulation plots for this op amp in the 0.25 μm CMOS process with all 0.25 μm channel length devices are shown next.

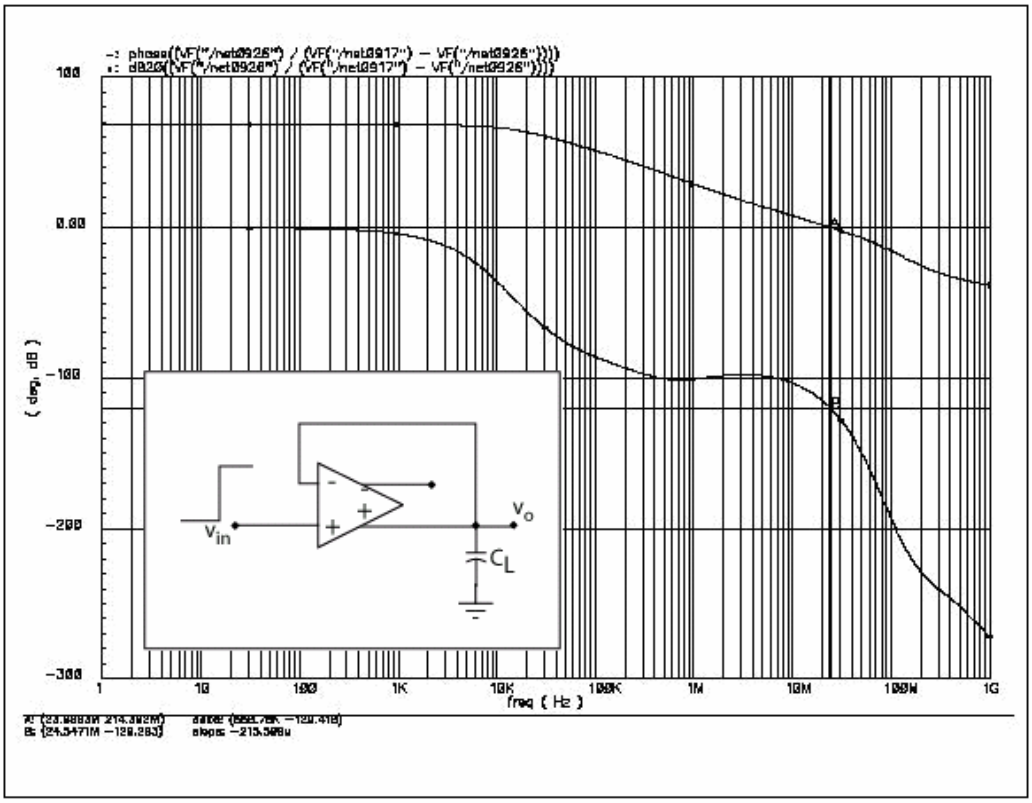


Figure 4.5. Small-signal simulation results for *OP*1 (single ended) in the 0.25 μm CMOS process

(Y axis: Magnitude in dB, Phase in degrees; X axis: Frequency in Hz)

A_v = 69 dB

Single-ended UGBW (single-ended CL = 2 pF) = 24 MHz

PM = 60 deg

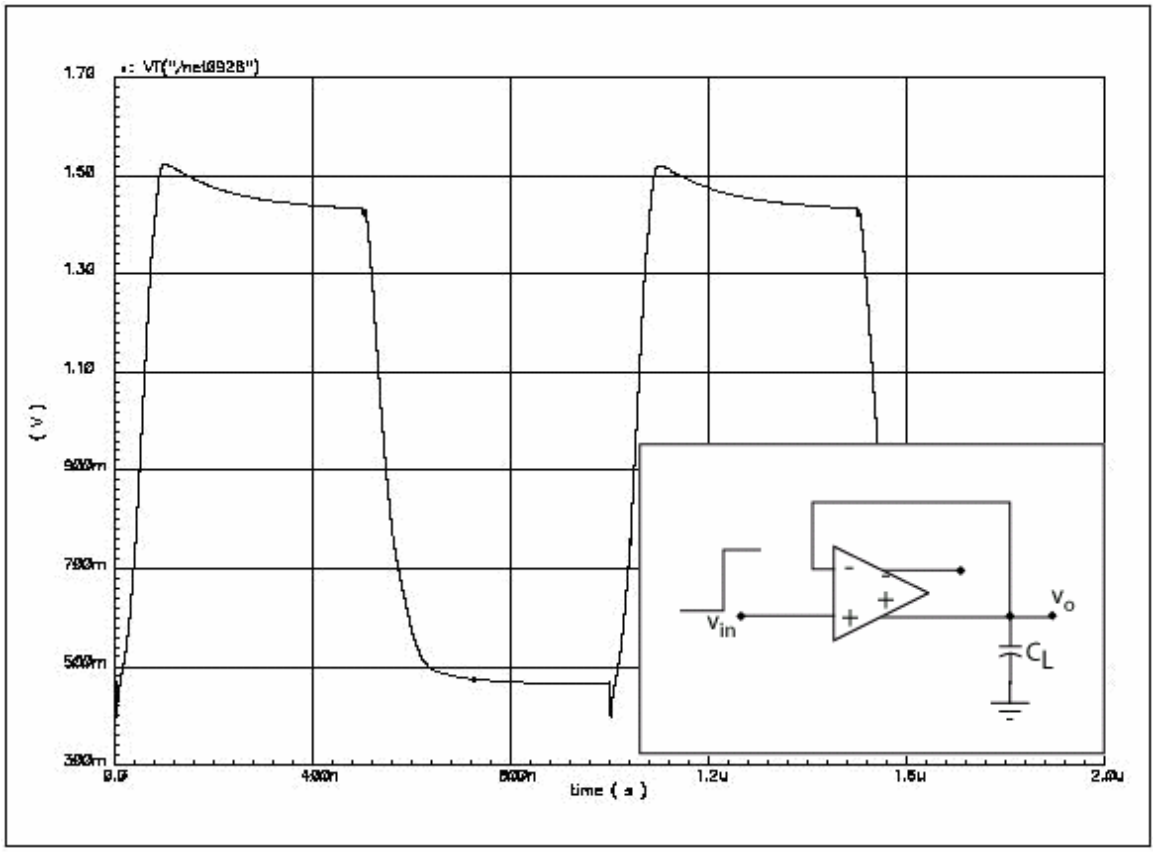


Figure 4.6. Large signal slewing of *OP*1 connected as a buffer with single-ended load capacitance of 2 pF in the 0.25 μm CMOS process

(Y axis: Volt; X axis: time)

$$SR^{+} = +16 \;\; V/\mu s \;\; , \quad SR^{-} = -12 \;\; V/\mu s$$

When a large signal input is applied, the output of the op amp tends to go beyond the limits of the input common-mode range because the negative resistance block (in Figure 4.4) tries to pull the outputs towards the supply rails. When this happens, the differential-in, differential-out gain block tries to suppress the

negative resistance block, and the output will finally settle to the limits of the input common-mode range.

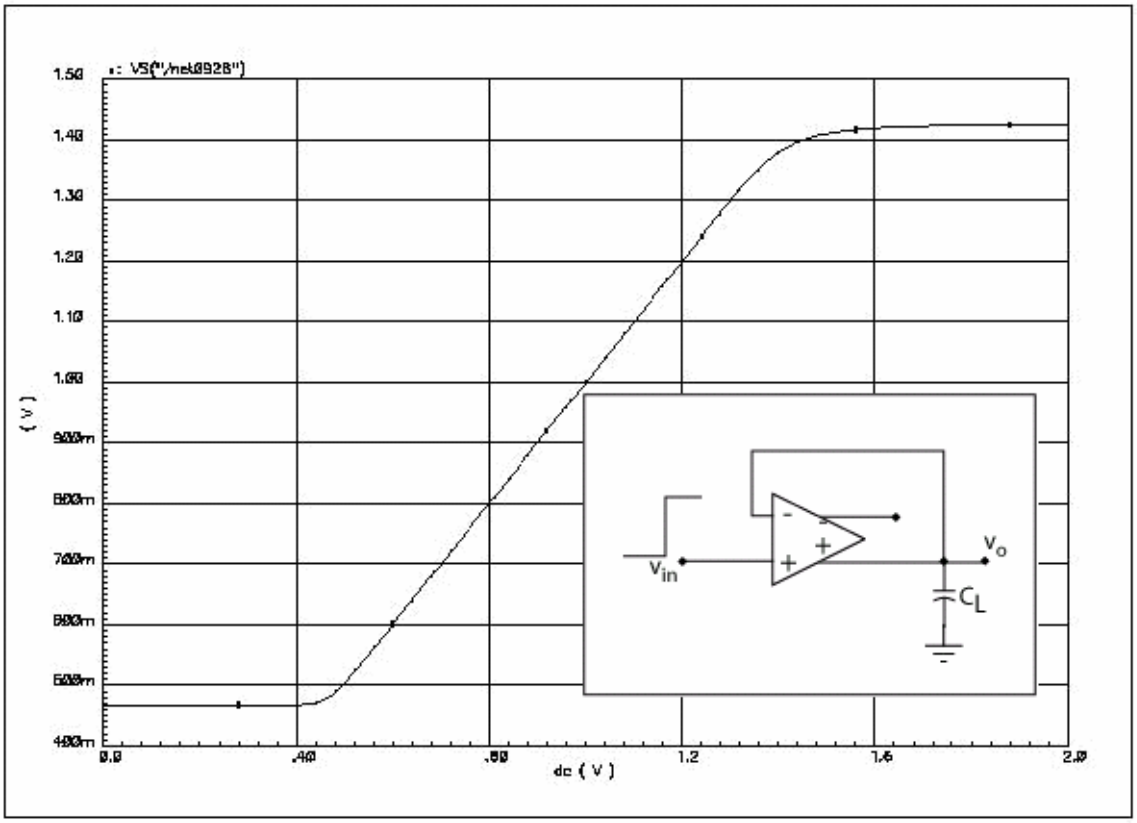


Figure 4.7. Input common-mode range of *OP*1 connected as a buffer in the 0.25 μm CMOS process

(Y axis: Output in Volt; X axis: Input in Volt)

ICMR = 0.468 – 1.424 V

Vdd = 2 V

The actual lower end of the ICMR for this op amp was 0.6 V, beyond which the NMOS device (M5 in Figure 4.4) in the first gain stage went into the linear region of operation.

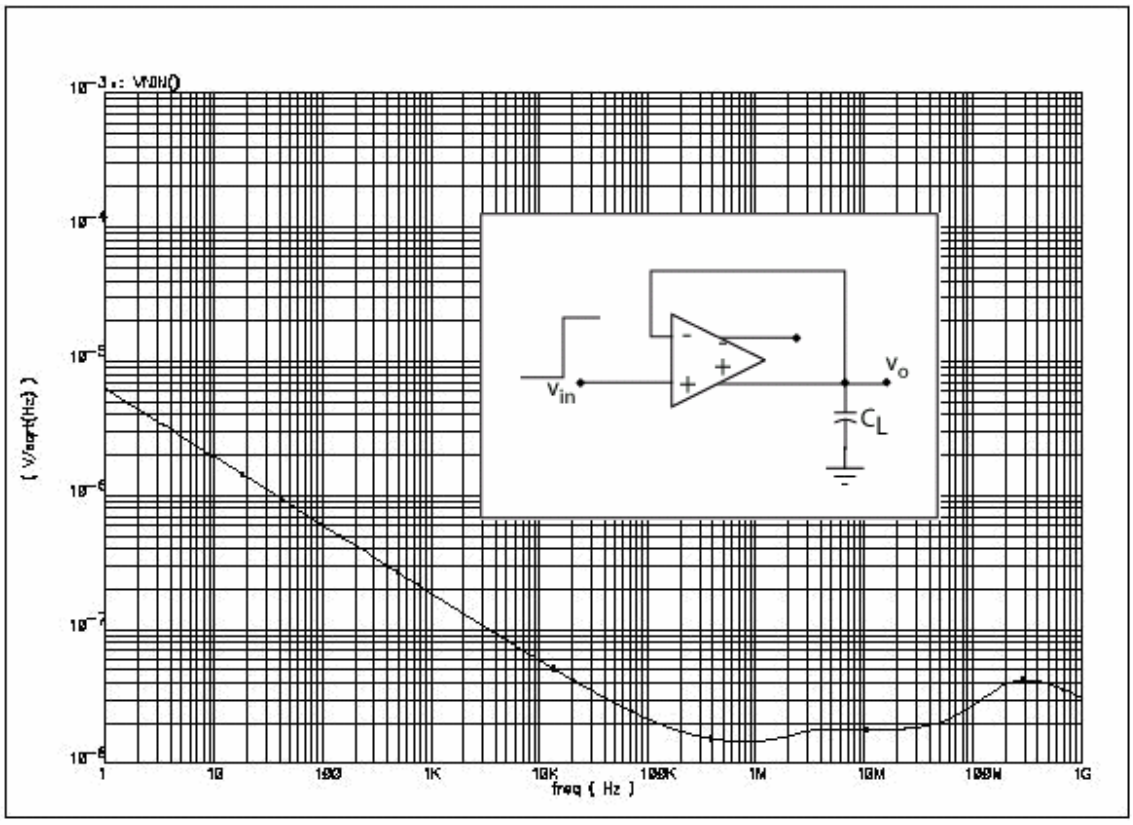


Figure 4.8. Input referred noise of *OP*1 connected as a buffer in the 0.25 μm CMOS process

(Y axis: Input referred noise in $V/\sqrt{Hz}$; X axis: Frequency in Hz)

For this op amp, the rms value of the input referred noise voltage was approximately 0.2 mV over a 100 MHz bandwidth.

4.6.3 Simulation Results of *OP*1 in the 0.18 μm CMOS Process

The simulated performance of *OP*1 in the 0.25 μm was shown in the previous section. In this section, its simulated performance in the 0.18 μm CMOS process with all 0.18 μm channel length devices is shown in Table 4.4. The op amp was again connected as a single-ended output, unity gain buffer.

Table 4.4. Simulated performance of *OP*1 in the 0.18 μm CMOS process

Performance specification	**Simulated value**
A_v	74 dB
UGBW (single-ended CL= 2 pF)	30 MHz
Phase margin	54 deg
Slew rate (single-ended CL= 2 pF)	+15, -13 $V / \mu s$
ICMR (Vdd = 1.5 V)	0.34 – 1.1 V
CMRR (at dc)	84 dB
PSRR (at dc)	78 dB
Input referred noise	2.5 $\mu V / \sqrt{Hz}$ (1 Hz) 0.3 $\mu V / \sqrt{Hz}$ (100 Hz) 12.7 $nV / \sqrt{Hz}$ (200 KHz: corner frequency)
Idd	700 μA

The simulation plots for this op amp in the 0.18 μm CMOS process with all 0.18 μm channel length devices are shown next.

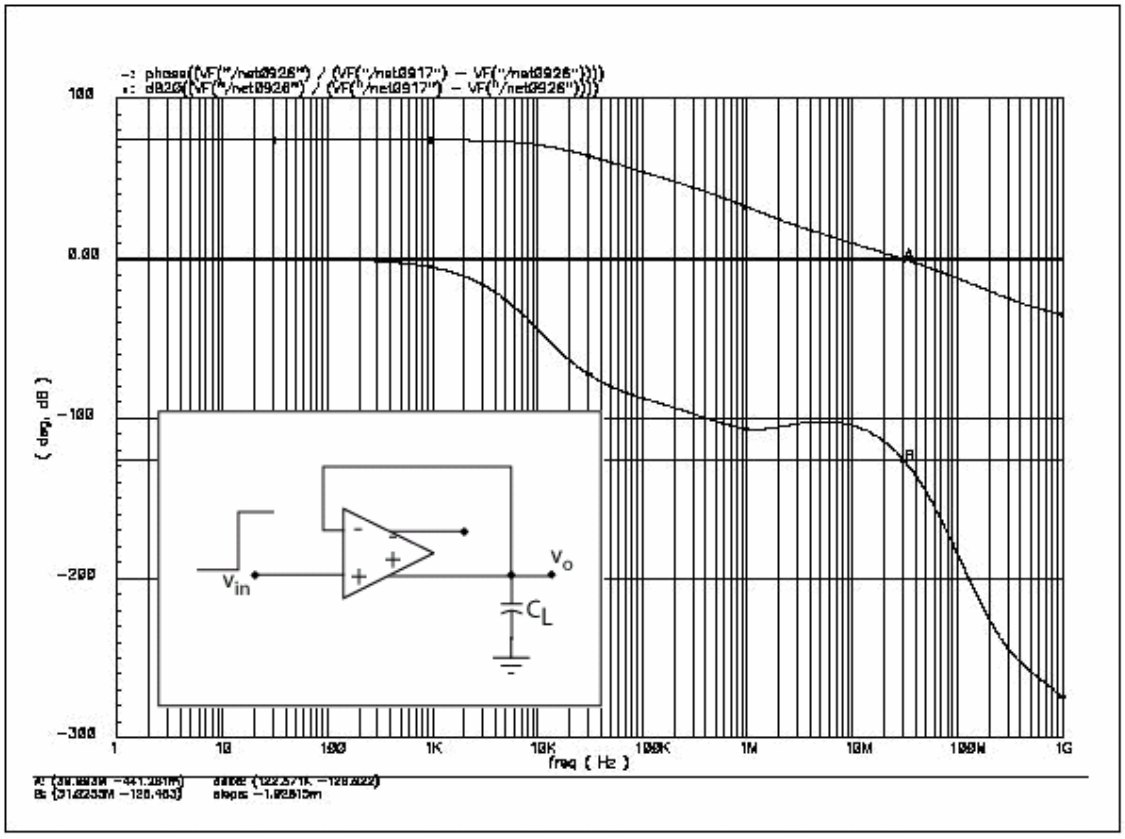


Figure 4.9. Small-signal simulation results for *OP*1 (single ended) in the 0.18 μm CMOS process

(Y axis: Magnitude in dB, Phase in degrees; X axis: Frequency in Hz)

A_v = 74 dB

Single-ended UGBW (single-ended CL = 2 pF) = 30 MHz

PM = 54 deg

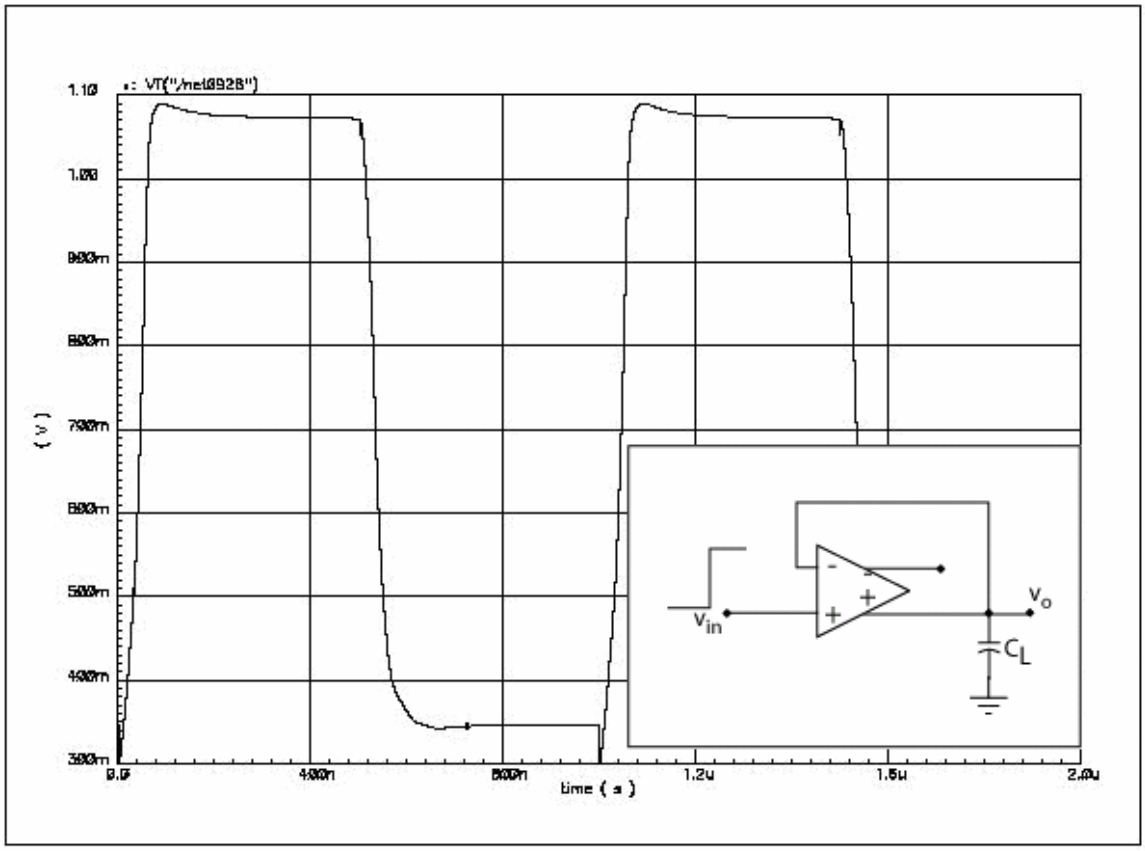


Figure 4.10. Slew rate of *OP*1 connected as a buffer with single-ended load capacitance of 2 pF in the 0.18 μm CMOS process

(Y axis: Output in Volt; X axis: time)

$SR^+ = +15 \;\; V/\mu s$

$SR^- = -13 \;\; V/\mu s$

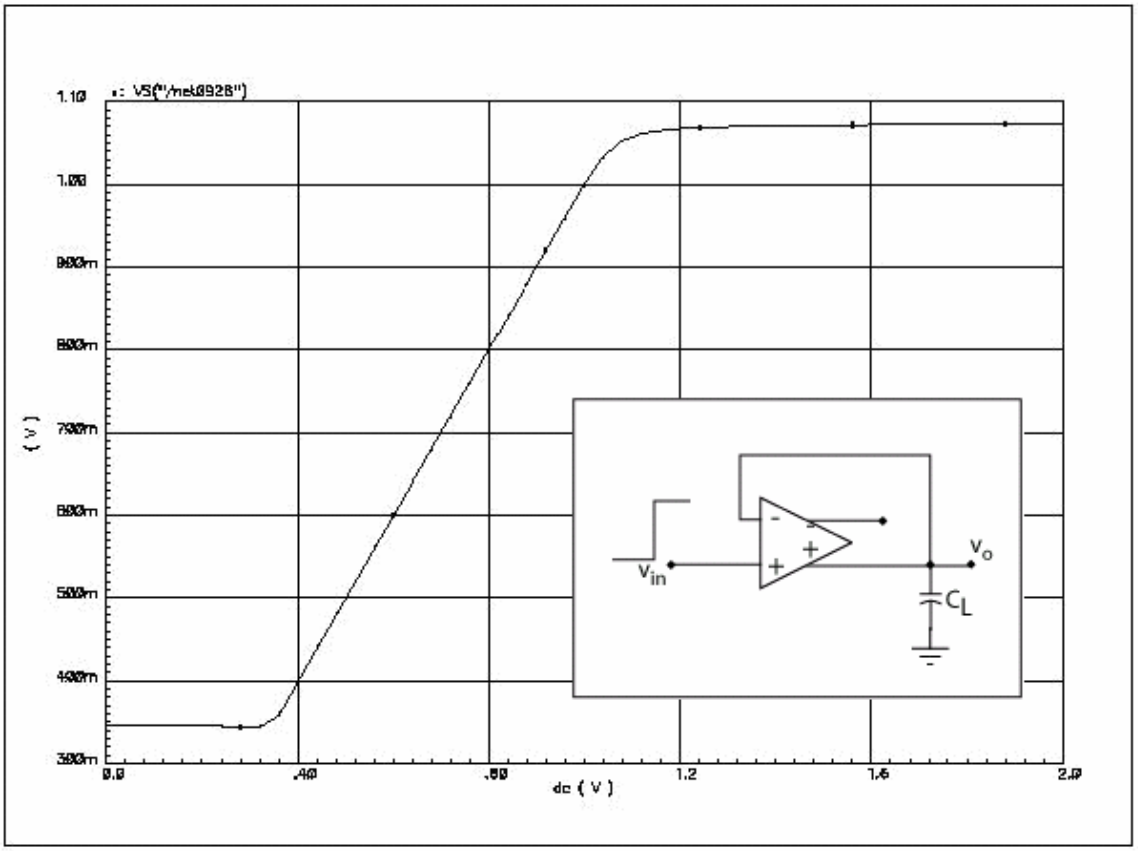


Figure 4.11. Input common-mode range of *OP*1 connected as a buffer in the 0.18 μm CMOS process

(Y axis: Output in Volt; X axis: Input in Volt)

ICMR = 0.34 – 1.1 V

Vdd = 1.5 V

The actual lower end of the ICMR for this op amp was 0.45 V, beyond which the NMOS device (M5 in Figure 4.4) in the first gain stage went into the linear region of operation.

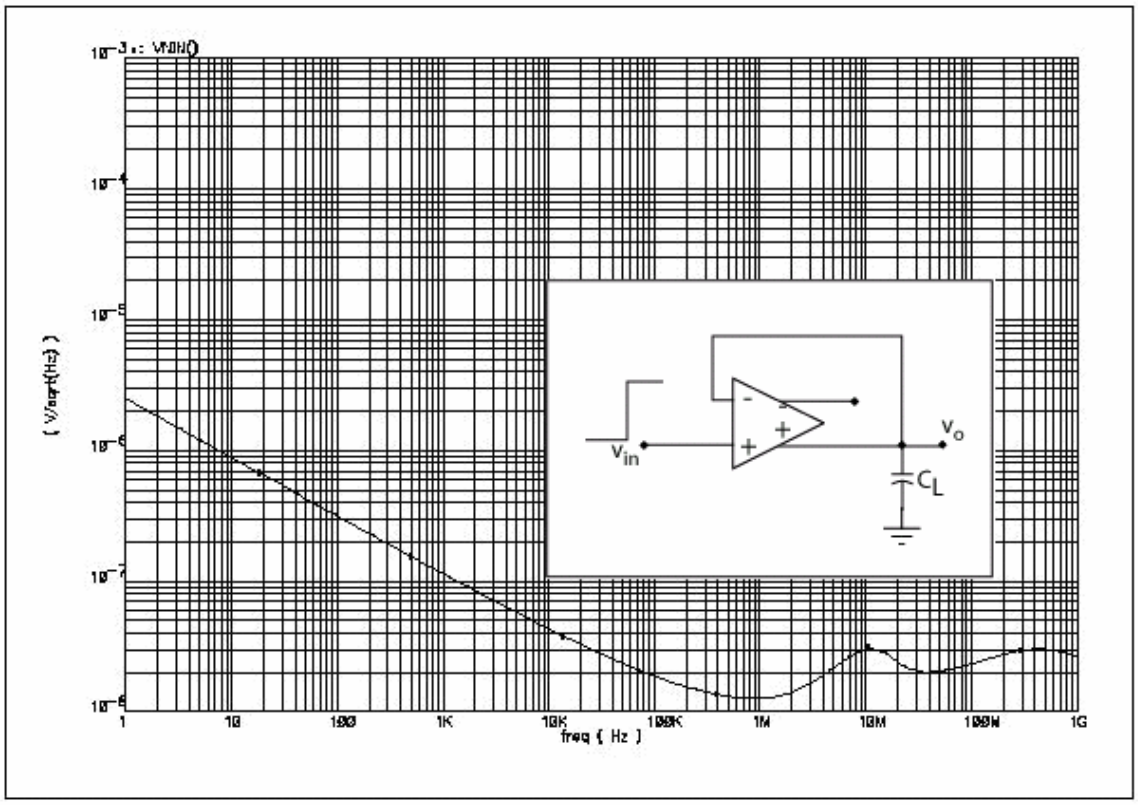


Figure 4.12. Input referred noise of *OP*1 connected as a buffer in the 0.18 μm CMOS process

(Y axis: Input referred noise in $V/\sqrt{Hz}$; X axis: Frequency in Hz)

For this op amp, the rms value of the input referred noise voltage was approximately 0.2 mV over a 100 MHz bandwidth.

4.6.4 Comparison of the Simulation Results of *OP*1 in Two Different CMOS Processes

The simulated performance for *OP*1 in the 0.25 μm CMOS process and the 0.18 μm CMOS process is tabulated next. The aspect ratios of the devices were maintained the same in both the processes with minimum feature-size channel length in each of these processes.

Table 4.5. Comparison of the simulated performance of *OP*1 in two different CMOS processes

Performance specification	**Simulated value**	
	0.25 μm CMOS	**0.18 μm CMOS**
Vdd	2 V	1.5 V
A_v	**69 dB**	**74 dB**
UGBW (single-ended CL=2 pF)	**24 MHz**	**30 MHz**
Phase margin	**60 deg**	**54 deg**
Slew rate (single-ended CL=2 pF)	+16, -12 $V / \mu s$	+15, -13 $V / \mu s$
ICMR	0.468 – 1.424 V	0.34 – 1.1 V
CMRR (at dc)	73 dB	84 dB
PSRR (at dc)	72 dB	78 dB
Input referred noise	6.28 $\mu V / \sqrt{Hz}$ (1 Hz) 14.7 $nV / \sqrt{Hz}$ (400 KHz: corner freq)	2.5 $\mu V / \sqrt{Hz}$ (1 Hz) 12.7 $nV / \sqrt{Hz}$ (200 KHz: corner freq)
Idd	817 μA	700 μA

The simulated performance of *OP*1 in two different CMOS processes is presented in Table 4.5. The maximum supply voltage in a process can be approximated as 10 times the minimum feature size. The supply voltages in the 0.25 μm CMOS process and the 0.18 μm CMOS process were kept at 2 V and 1.5 V respectively. This op amp was designed to achieve:

- Constant small-signal gain

It was designed for an overall single-ended small-signal gain of 20,000 (86 dB), but its simulated value was less due to the degrading bulk effects, which decreased the small-signal gain. The small-signal gain was expressed in Equation (3.21). Bulk effects degraded (increased) the denominator of Equation (3.21), which resulted in decrease in the small-signal gain. The variation in the small-signal gain was 5 dB across both the technologies. It can be seen from Equation (3.21), the small-signal gain is directly proportional to the input transconductance. The transconductance in the 0.18 μm CMOS process was slightly larger than its value in the 0.25 μm CMOS process, which gave a larger small-signal gain in the former process.

- Constant phase margin across different technologies.

The phase margin was designed as 78.6 degrees with 5 times the bias current in the second gain stage as compared to the first gain stage. The phase margin was degraded by the fact that the ratio of the bias currents in the two gain stages was less than 5; the design was ideally made for this ratio to have a value of 5. This ratio of the bias currents was approximately 4 and 3 in the 0.25 μm

CMOS process and the 0.18 μm CMOS process respectively. The designed aspect ratios of the devices could not ensure a ratio of 5 in both the processes due to limits of bulk drive in the biasing circuit.

As it was stated earlier, the UGBW frequency will be different across different technologies, and it can be seen in Table 4.5. The variation in the UGBW frequency is dependent on the transconductance of the input transistors, which depend on the *technology-dependent* parameters. Considering the slew rates, although a constant bias current generation scheme was used, the magnitude of the bias currents in both the technologies was different, which resulted in slightly varied slew rates. The input common-mode range, CMRR, PSRR, and the input referred noise were dependent on the *technology-dependent* parameters, and they were different in both the technologies. Thus, overall, this design did result in an almost constant gain and phase margin with known limiting reasons for their degradation. In the following section, the simulation results for the op amp *OP2* with all minimum feature-size channel length devices are presented.

4.6.5 Simulation Results of Op Amp *OP*2

In this section, the simulation results for the op amp *OP*2 are presented. This op amp is a two-stage op amp with all $L_{\min}$ -based devices and maximum gain. The gain stage of *OP2* is shown in Figure 3.10. It was designed to drive a maximum differential load capacitance of 1 pF. This op amp was fabricated in two different CMOS processes to verify technology-independent phase margin. The minimum feature-size channel length was used in both of these technologies. The architecture of the gain stage of this op amp is shown in Figure 3.10, which is again redrawn below in Figure 4.13.

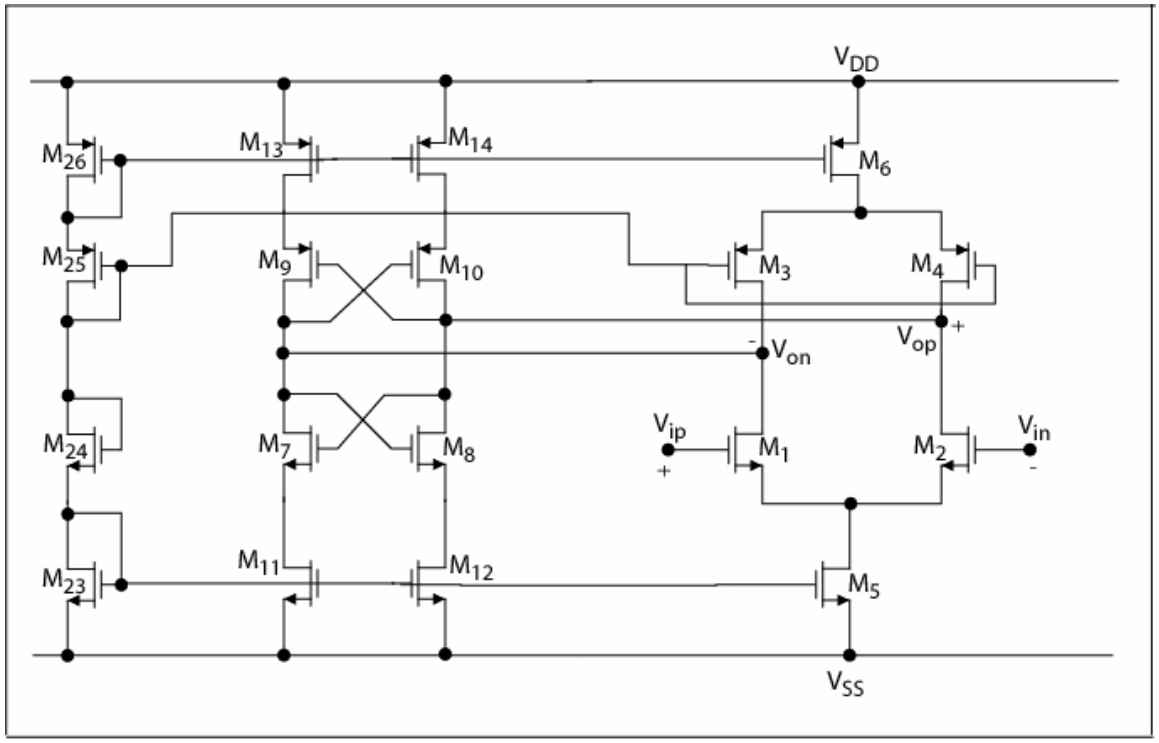


Figure 4.13. Gain stage of the op amp *OP*2

4.6.6 Simulation Results of *OP2* in the 0.25 μm CMOS Process

The simulation results for *OP*2 in the 0.25 μm CMOS process with 0.25 μm channel length devices are presented first. The op amp was connected as a single-ended output, unity gain buffer.

Table 4.6. Simulated performance of *OP*2 in the 0.25 μm CMOS process

Performance specification	**Simulated value**
Vdd	2 V
A_v	71 dB
UGBW (single-ended CL= 2 pF)	26 MHz
Phase margin	60 deg
Slew rate (single-ended CL= 2 pF)	+17, -12 $V / \mu s$
ICMR	0.46 – 1.4 V
CMRR (at dc)	74 dB
PSRR (at dc)	73 dB
Input referred noise	6.2 $\mu V / \sqrt{Hz}$ (1 Hz) 0.6 $\mu V / \sqrt{Hz}$ (100 Hz) 13 $nV / \sqrt{Hz}$ (400 KHz: corner frequency)
Idd	800 μA

The simulation plots for this op amp in the 0.25 μm CMOS process with all 0.25 μm channel length devices are shown next.

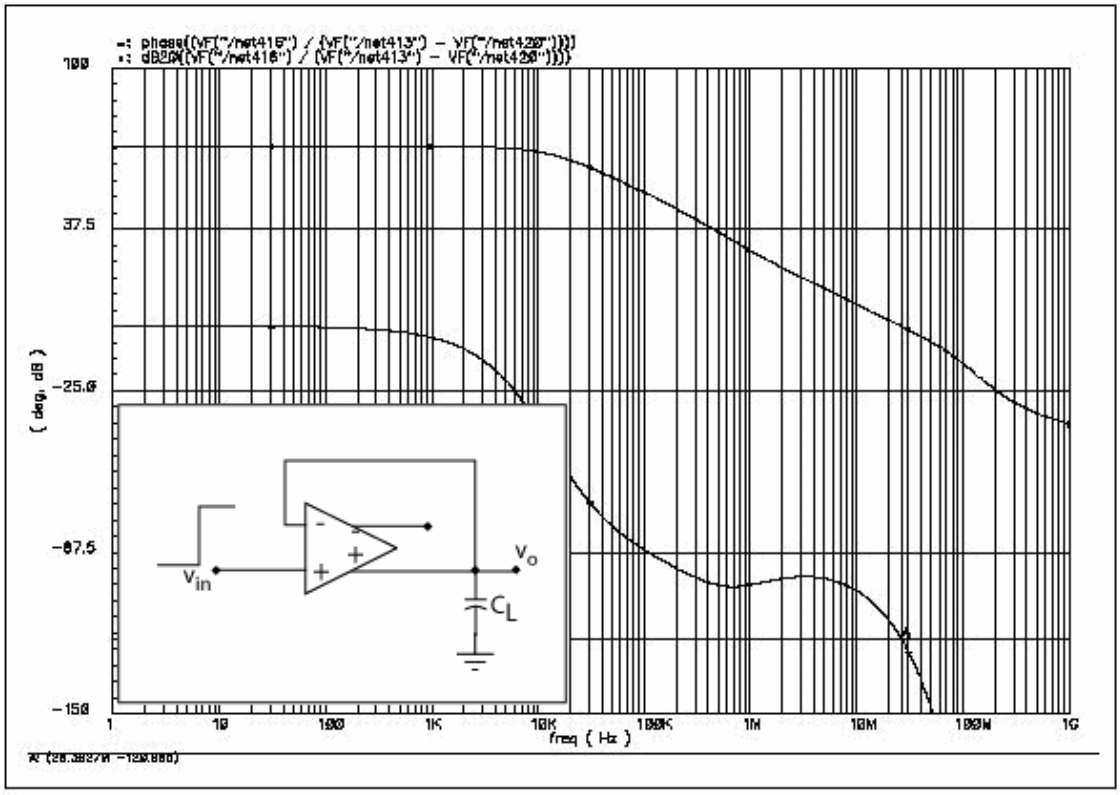


Figure 4.14. Small-signal simulation results of *OP*2 (single-ended) in the 0.25 μm CMOS process

(Y axis: Magnitude in dB, Phase in degrees; X axis: Frequency in Hz)

A_v = 71 dB

Single-ended UGBW (single-ended CL 2 pF) = 26 MHz

PM = 60 deg

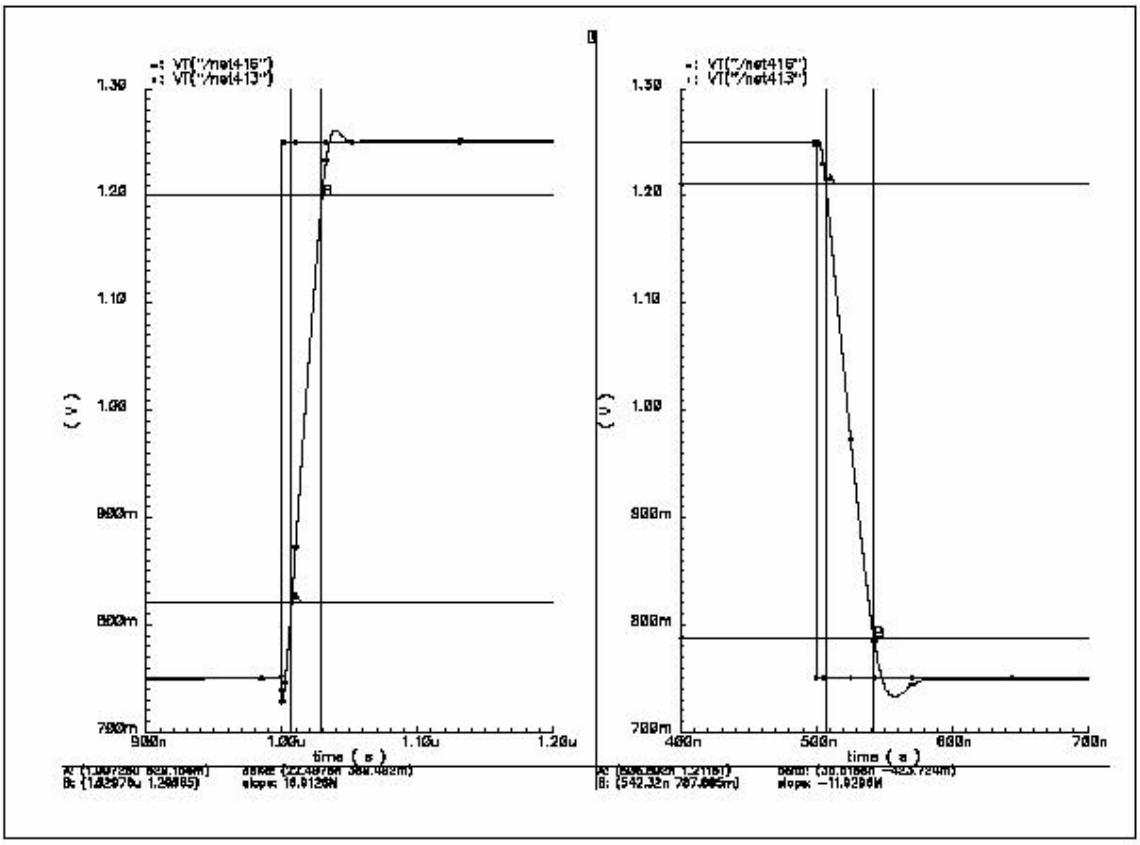


Figure 4.15. Slew rate of *OP*2 connected as a buffer with single-ended load capacitance of 2 pF in the 0.25 μm CMOS process

(Y axes: Output in Volt; X axes: time)

$SR^{+} = +17 \;\; V / \mu s$

$SR^{-} = -12 \;\; V / \mu s$

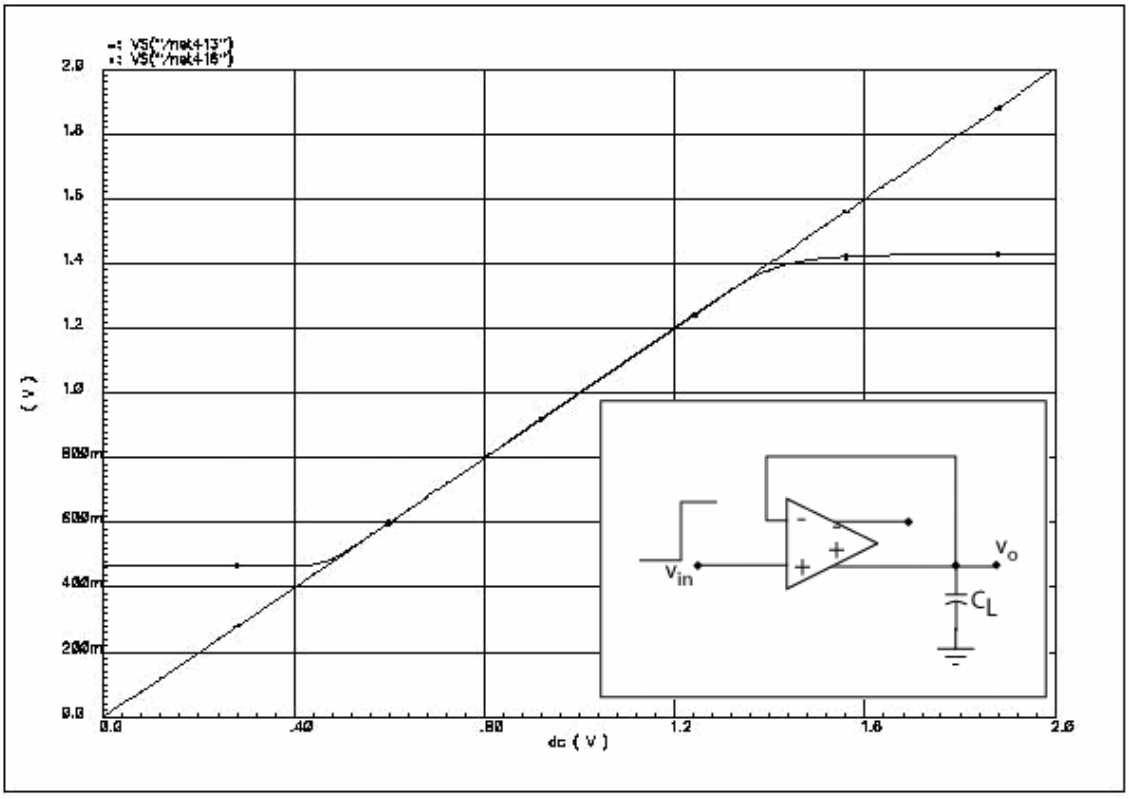


Figure 4.16. Input common-mode range of *OP*2 connected as a buffer in the 0.25 μm CMOS process

(Y axis: Output in Volt; X axis: Input in Volt)

ICMR = 0.46 – 1.4 V

Vdd = 2 V

The actual lower end of the ICMR for this op amp was 0.6 V, beyond which the NMOS device (M5 in Figure 4.13) in the first gain stage went into the linear region of operation

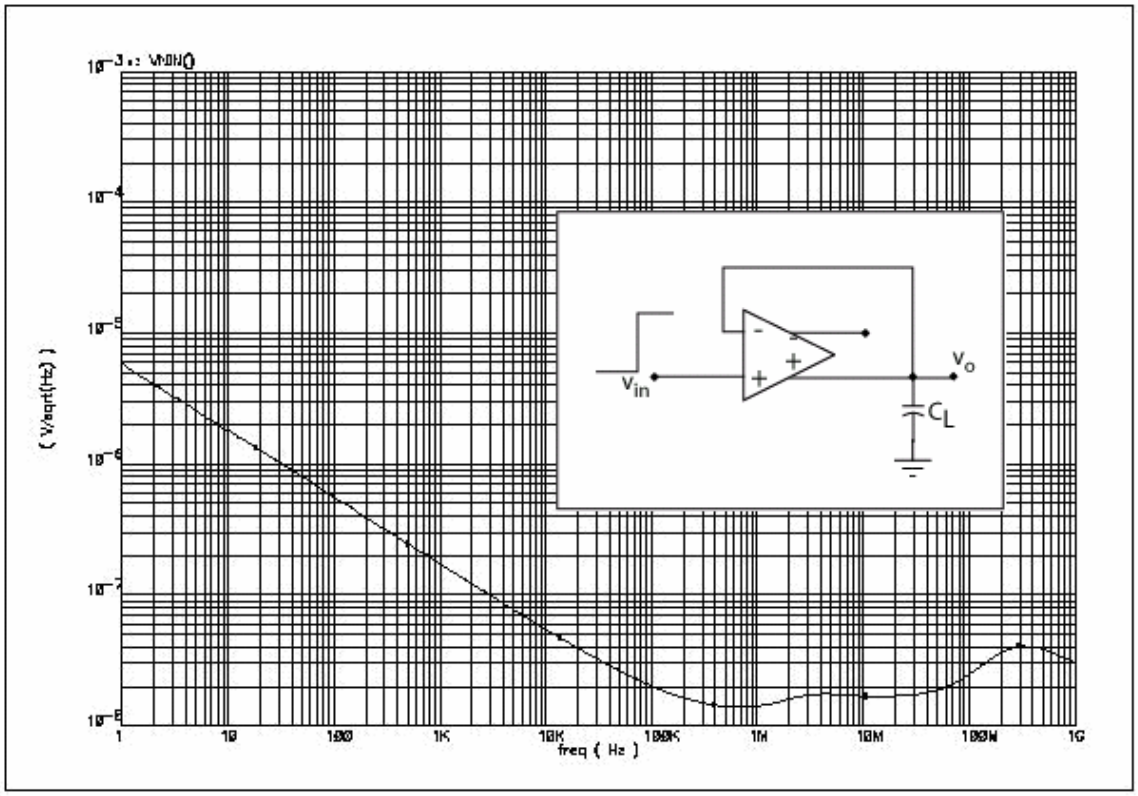


Figure 4.17. Input referred noise of *OP*2 connected as a buffer in 0.25 μm CMOS process

(Y axis: Input referred noise in $V/\sqrt{Hz}$; X axis: Frequency in Hz)

4.6.7 Simulation Results of *OP2* in the 0.18 μm CMOS Process

The simulation results for *OP*2 in the 0.18 μm CMOS process with 0.18 μm channel length devices are presented next. The op amp was connected as single-ended output, unity gain buffer.

Table 4.7. Simulated performance of *OP*2 in the 0.18 μm CMOS process

Performance specification	**Simulated value**
Vdd	1.5 V
A_v	75 dB
UGBW (single-ended CL= 2 pF)	40 MHz
Phase margin	50 deg
Slew rate (single-ended CL= 2 pF)	+21, -17 $V / \mu s$
ICMR	0.37 – 1.1 V
CMRR	84 dB
PSRR	86 dB
Input referred noise	2.2 $\mu V / \sqrt{Hz}$ (1 Hz) 0.3 $\mu V / \sqrt{Hz}$ (100 Hz) 11 $nV / \sqrt{Hz}$ (300 KHz: corner frequency)
Idd	750 μA

The simulation plots for this op amp in the 0.18 μm CMOS process with all 0.18 μm channel length devices are shown next.

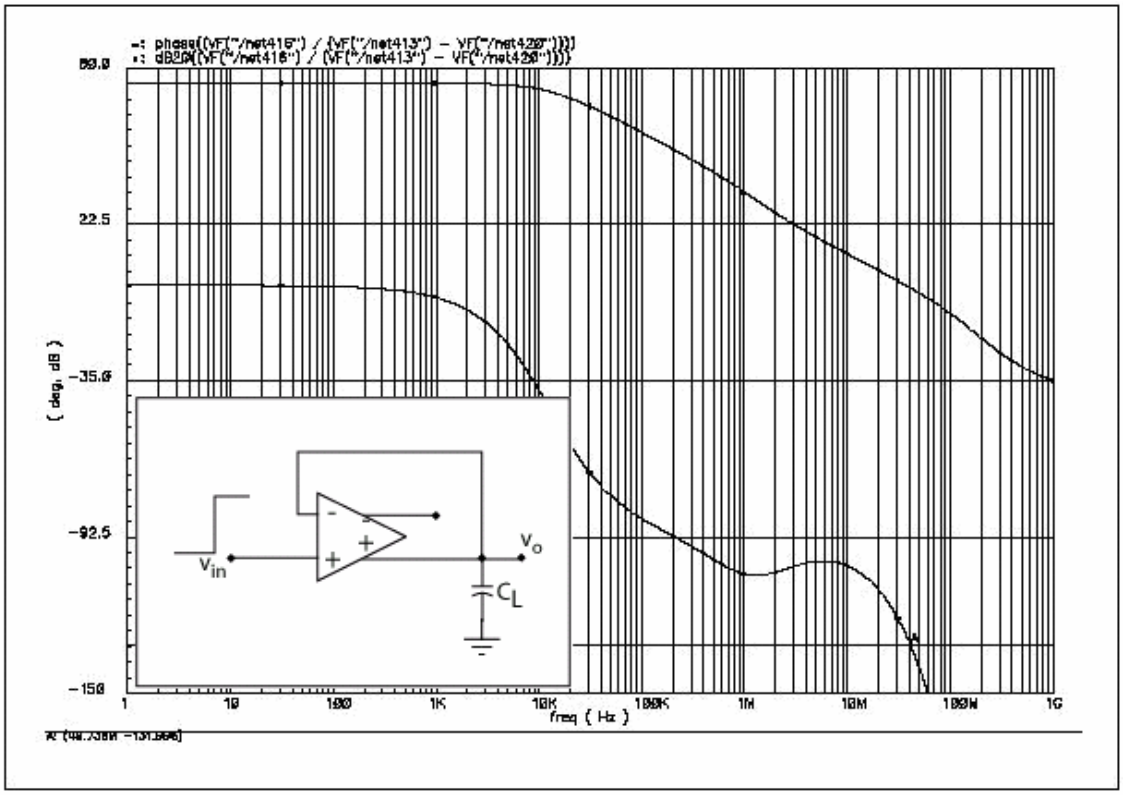


Figure 4.18. Small-signal simulation results of *OP*2 (single ended) in the 0.18 μm CMOS process

(Y axis: Magnitude in dB, Phase in degrees; X axis: Frequency in Hz)

A_v = 75 dB

UGBW (single-ended CL = 2 pF) = 40 MHz

PM = 50 deg

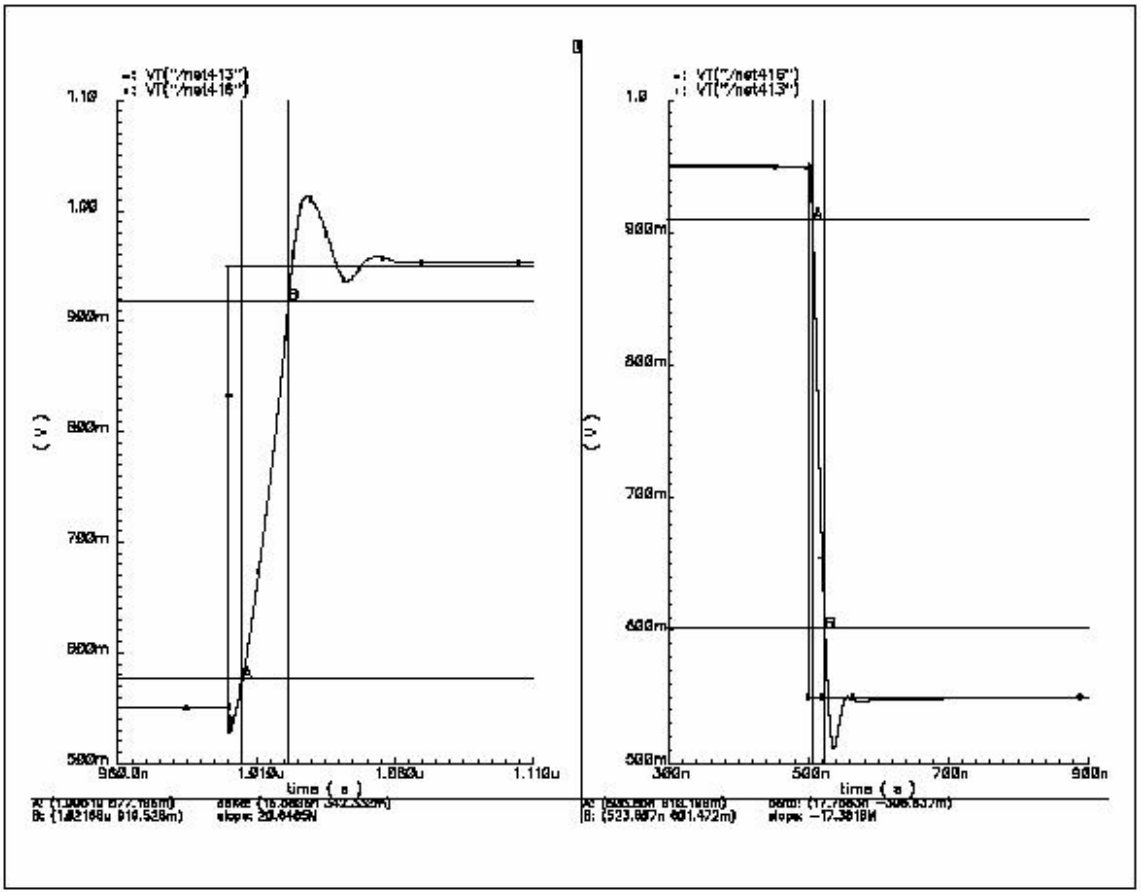


Figure 4.19. Slew rate of *OP*2 connected as a buffer with single-ended load capacitance of 2 pF in the 0.18 μm CMOS process

(Y axes: Output in Volt; X axes: time)

$SR^{+} = +21 \;\; V / \mu s$

$SR^{-} = -17 \;\; V / \mu s$

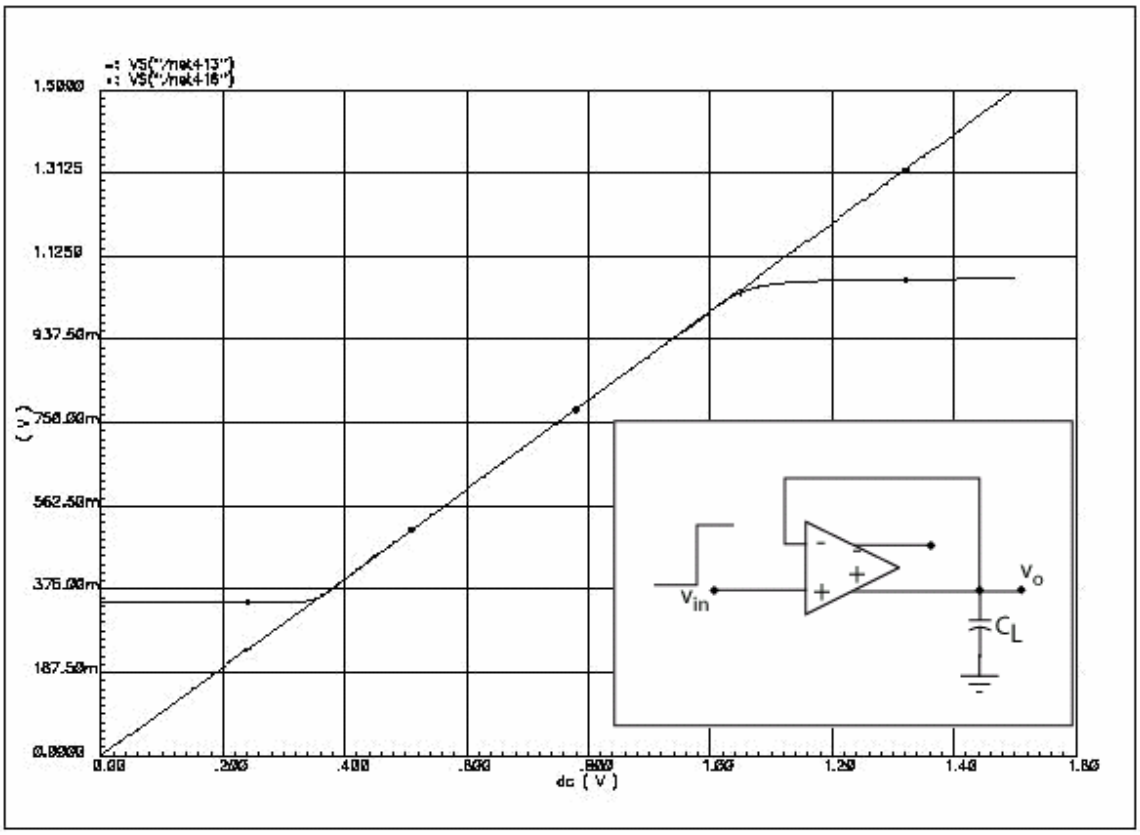


Figure 4.20. Input common-mode range of *OP*2 connected as a buffer in the 0.18 μm CMOS process

(Y axis: Output in Volt; X axis: Input in Volt)

ICMR = 0.37 – 1.1 V

Vdd = 1.5 V

The actual lower end of the ICMR for this op amp was 0.5 V, beyond which the NMOS device (M5 in Figure 4.13) in the first gain stage went into the linear region of operation

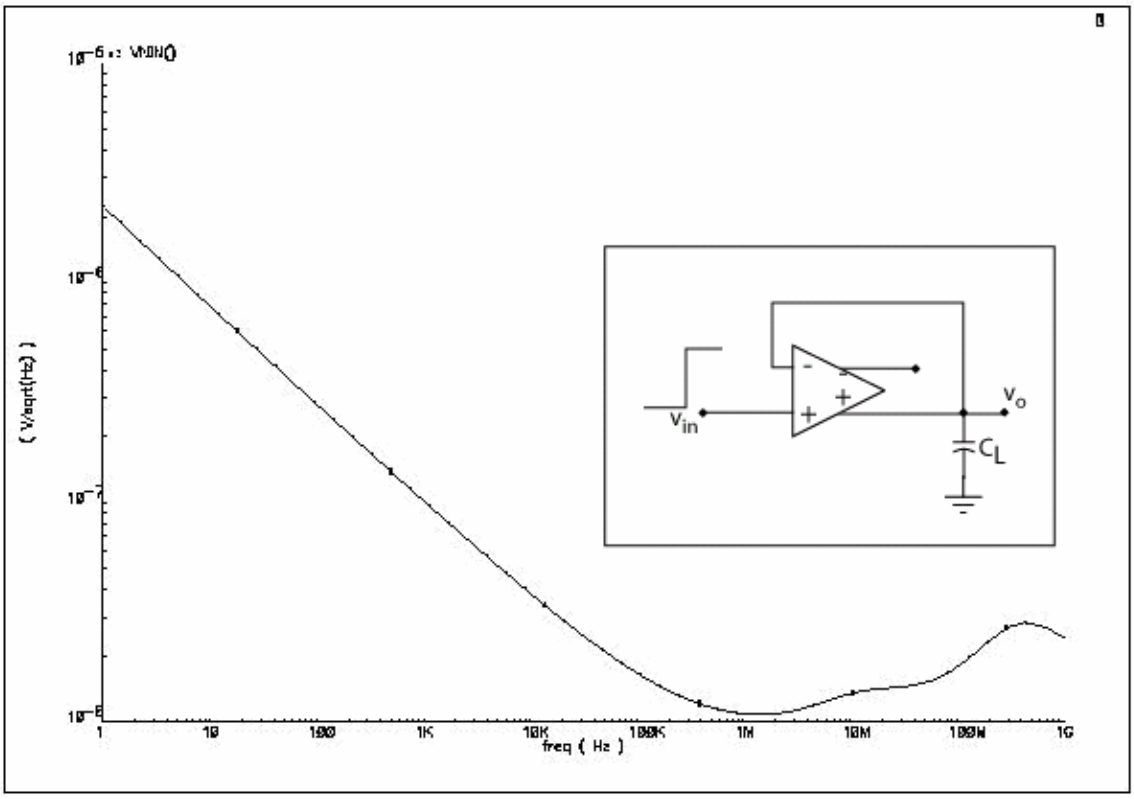


Figure 4.21. Input referred noise of *OP*2 connected as a buffer in the 0.18 μm CMOS process

(Y axis: Input referred noise in $V/\sqrt{Hz}$; X axis: Frequency in Hz)

4.6.8 Comparison of the Simulated Performance of *OP2* in Two different CMOS Processes

The following table compares the simulated performance of *OP*2 in both the CMOS processes.

Table 4.8. Comparison of the simulated performance of *OP*2 in the 0.25 μm CMOS and the 0.18 μm CMOS processes

Performance specification	**Simulated value**	
	0.25 μm CMOS	**0.18 μm CMOS**
Vdd	2 V	1.5 V
A_v	**71 dB**	**75 dB**
UGBW (single-ended CL= 2 pF)	**26 MHz**	**40 MHz**
Phase margin	**60 deg**	**50 deg**
Slew rate (single-ended CL= 2 pF)	+17, -12 $V/\mu s$	+21,-17 $V/\mu s$
ICMR	0.46 – 1.4 V	0.37 – 1.1 V
CMRR (at dc)	74 dB	84 dB
PSRR (at dc)	73 dB	86 dB
Input referred noise	6.2 $\mu V/\sqrt{Hz}$ (1 Hz) 13 $nV/\sqrt{Hz}$ (400 KHz: corner freq)	2.2 $\mu V/\sqrt{Hz}$ (1 Hz) 11 $nV/\sqrt{Hz}$ (300 KHz: corner freq)
Idd	800 μA	750 μA

It was expected that the gain of this op amp will be larger than *OP*1, but it was small due to the degrading bulk effects, which decreased the small-signal gain. The phase margin was also less than expected, and it varied in both the technologies because the ratios of the bias currents in the two gain stages of the op amp were not constant. The phase margin is indirectly related to the forward biasing of the PMOS bulk diodes. The threshold voltage modulation of the PMOS devices through their bulk drive was more successful in the 0.25 μm CMOS process than in the 0.18 μm CMOS process. This happened because the former process had a larger value of the nominal threshold voltage. It is easier to modulate the threshold voltage considerably through bulk drive if its nominal value is large enough. For a small nominal value of the threshold voltage, the bulk drive will only cause small changes in the threshold voltage from the nominal value. In the 0.18 μm CMOS process, the nominal threshold voltage was less, and further reduction of the threshold voltage through bulk drive was limited. This resulted in smaller bias current in the second gain stage in the 0.18 μm CMOS process, and it caused a reduced phase margin. Other performance specifications also changed as most of them depend on the *technology-dependent* parameters.

4.7 Measurement Results

The simulation results, shown in the previous section, showed that an op amp, capable of achieving large small-signal gain and constant phase margin with all minimum feature-size channel length devices, can be designed and easily migrated across different CMOS processes. The same results were also expected through measurements, but various limitations during fabrication and testing limited the performance of the op amp, and they will be discussed in detail in the following sections.

During the fabrication process, use of minimum feature size channel length devices pushes the lithographic process to its edge, which results in irregularities in the channel lengths of different devices. So, input offset voltage of the op amp will be a critical specification that will be effected by the use of small channel length devices. While using small channel lengths, it is important to have relevant information about the possible mismatches in fabrication for the used channel lengths.

4.7.1 Measurement Results for Matching of Devices

In this section, the mismatches in currents of a simple NMOS current mirror, shown in Figure 4.13, with minimum channel length devices are presented. The aspect ratios of both the NMOS transistors in this figure were kept the same for 1:1 current mirroring. If the voltages V_1 and V_2 are equal, then the

mismatches in the device geometries of both the transistors will correspond to the mismatch in I_1 and I_2.

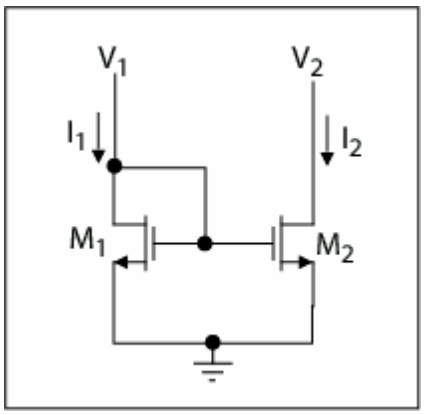


Figure 4.22. Simple NMOS current mirror

The MOSFETs in the op amps (*OP*1 and *OP*2) are operated in weak inversion. The drain current in the input devices can be approximated as

$$I = I_0 e^{\frac{V_{gs}}{nV_t}} \tag{4.30}$$

where, V_t is the thermal voltage, and n is the sub-threshold slope of the MOSFETs ($1.5 < n < 2.5$).

From Equation (4.30), we get

$$V_{gs} = nV_t \ln\left(\frac{I}{I_0}\right) \tag{4.31}$$

Referring to Figure 4.13, the offset voltage can be given as

$$V_{os} = \left|V_{gs1} - V_{gs2}\right| = \left|nV_t \ln\left(\frac{I_1}{I_2}\right)\right| \tag{4.32}$$

The above expression can be used to calculate the offset voltage when the mismatch in the values of I_1 and I_2 are known. The measurement data for the mismatches in I_1 and I_2 in Figure 4.22 are presented next. The p-substrate of the NMOS transistors (substrate voltage denoted by V_{sub} in the following tables) were forward and reversed biased to observe its effect on matching of I_1 and I_2. The aspect ratio (W/L) of both the transistors was $20\mu m / 0.25\mu m$.

Table 4.9. Mismatches in I_1 and I_2 for $V_{sub} = 0$ V in the 0.25 μm CMOS process

V1 (V)	V2 (V)	I1 (uA)	I2 (uA)	mismatch %
0.44863	0.44868	1.77	1.75	-1.14
0.4856	0.48567	4.769	4.771	0.04
0.50292	0.5031	7.45	7.37	-1.08
0.56695	0.56685	33.116	33.72	1.79
0.59503	0.59465	55.76	56.99	2.15
0.6349	0.63408	95.79	98.09	2.34

Table 4.10. Mismatches in I_1 and I_2 for $V_{sub} = 0.3$ V (forward biased) in the 0.25 μm CMOS process

V1 (V)	V2 (V)	I1 (uA)	I2 (uA)	mismatch %
0.33934	0.33935	0.7315	0.7324	0.12
0.38759	0.38762	2.595	2.604	0.34
0.44915	0.44912	11.092	11.292	1.77
0.47212	0.47209	18.22	18.52	1.61
0.54403	0.5432	66.4	68.26	2.72
0.5754	0.5739	105.11	108.24	2.89

Table 4.11. Mismatches in I_1 and I_2 for $V_{sub} = 0.5$ V (forward biased) in the 0.25 μm CMOS process

V1 (V)	V2 (V)	I1 (uA)	I2 (uA)	mismatch %
0.28875	0.28875	1.232	1.251	1.51
0.38867	0.38855	11.553	11.851	2.51
0.4396	0.43918	30.761	31.658	2.83
0.50465	0.50351	96.04	98.67	2.66
0.52542	0.52394	125.51	128.93	2.65

In all the above mismatch measurements, the data for very low values of the currents (< 5 uA) were not reliable due to limitations of the current measuring equipment. It was observed that for a given magnitude of the currents, forward biasing the bulks did not significantly improve matching.

From the mismatch data in the 0.25 μm CMOS process, let us assume the maximum value of mismatch in I_1 and I_2 to be 3 %. Also, let the worst-case value of n be 3. Then from Equation (7.3), the value of the offset voltage will be

$$V_{os} = \left|V_{gs1} - V_{gs2}\right| = \left|nV_t \ln\left(\frac{I_1}{I_2}\right)\right| = 2.3 \text{ mV} \tag{4.33}$$

So, the offset voltage given in Equation (4.33) can give us an estimation of the magnitude of the offset voltage for the op amp $OP2$ fabricated in the 0.25 μm CMOS process. The overall offset voltage will be larger than the value approximated above due to the finite gain of the first gain stage, and the offset contribution from the later stages will also increase the overall offset voltage. The actual measurements of the offset voltage of $OP2$ are presented in the later sections.

For the current mirror in Figure 4.22, the same mismatch measurements were made in a 0.18 μm CMOS process, and the mismatch data is presented next. The aspect ratio of the NMOS device was $10\mu m / 0.18\mu m$.

Table 4.12. Mismatches in I_1 and I_2 for $V_{sub} = 0$ V in the 0.18 μm CMOS process

Vsub=0				
V1 (V)	V2 (V)	I1 (uA)	I2 (uA)	mismatch %
0.3393	0.3486	6.527	5.354	17.97
0.3566	0.3699	10.04	8.34	16.93
0.369	0.3864	14.09	11.83	16.03
0.3786	0.3993	18.43	15.7	14.81
0.3879	0.4126	22.81	19.52	14.42

Table 4.13. Mismatches in I_1 and I_2 for $V_{sub} = 0.3$ V (forward biased) in the 0.18 μm CMOS process

Vsub=0.3				
V1 (V)	V2 (V)	I1 (uA)	I2 (uA)	mismatch %
0.3118	0.3233	9.48	7.99	15.71
0.3272	0.3423	13.2	11.2	15.15
0.3404	0.3587	17.16	14.72	14.21
0.3503	0.3709	21.47	18.66	13.08
0.3609	0.3842	25.71	22.48	12.56

The first clear observation is that the mismatch in the 0.18 μm CMOS process was much larger than in the 0.25 μm CMOS process. As stated earlier in Equation (2.8) in Chapter 2, for extremely small channel lengths, the mean-square

mismatch is inversely proportional to the square of the channel length. Thus, when migrating from the 0.25 μm CMOS process to the 0.18 μm CMOS process, the device dimensions (both W and L) were scaled down by a factor of almost 1.4, and the corresponding mismatch should worsen by a factor of almost 1.66 (which is $(1.4)^{3/2}$). This assumes that the capability to match the devices is identical in both the CMOS processes. Comparing the two CMOS processes, it will always be difficult to match a device with 0.18 μm channel length in the 0.18 μm CMOS process with a device with 0.25 μm channel length in the 0.25 μm CMOS process. From the mismatch data in Tables 4.9 through 4.13, the mismatch in the 0.18 μm CMOS process was almost 5 times worse than the mismatch in the 0.25 μm CMOS process. This shows that while migrating from the 0.25 μm CMOS process to the 0.18 μm CMOS process, even though we expected the mismatch to worsen by a factor of 1.66, it was worse by a factor of 5. This suggests that the 0.18 μm CMOS process had worse matching than the 0.25 μm CMOS process.

To estimate the offset voltage in the 0.18 μm CMOS process, let us assume the maximum value of mismatch in I_1 and I_2 to be 15 %. Also, let the worst-case value of n be 3. Then from Equation (7.3), the maximum value of the offset voltage would be

$$V_{os} = 11 \text{ mV} \tag{4.34}$$

This gives us an initial estimate for the input offset voltage of the op amp. The actual data for the input offset voltage is presented later in this chapter.

4.7.2 Bias Current Measurements

As explained earlier in the previous chapter (Figure 3.11), an adaptive PMOS bulk drive scheme was used to generate the bias currents in the op amps. For the purpose of understanding, this biasing scheme is redrawn below in Figure 4.23.

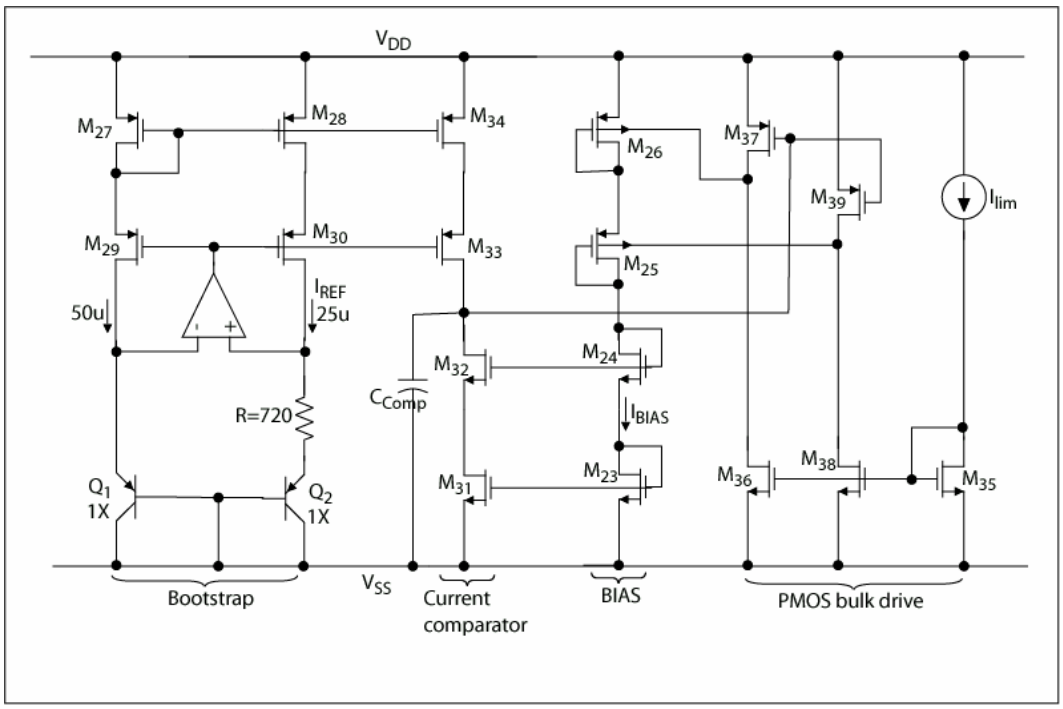


Figure 4.23. Bias current generation circuit using adaptive PMOS bulk drive

In Figure 4.23, any ripple in V_{DD} will directly effect the V_{gs} of the stacked, diode-connected transistors M_{23} through M_{26}. These transistors are big enough so that they operate in weak inversion. In absence of any PMOS bulk drive, it can be seen that any change in V_{gs} of these four transistors will cause an exponential

change in the value of I_{BIAS}, which is highly undesirable. But, in presence of the PMOS bulk drive, this current will tend to remain fairly constant over a range of V_{DD} for which the bulk drive will work satisfactorily. The measurement data showing the variation of the normalized I_{BIAS} with V_{DD} in the 0.25 μm CMOS process is shown next in Figure 4.24. The normalized I_{BIAS} refers to the value of I_{BIAS} normalized to the reference current in the Bootstrap circuit (whose nominal value was $27\,\mu A$). As it can be seen in Figure 4.24, the measured and the simulated data for I_{BIAS} had the same characteristics and closely resembled each other.

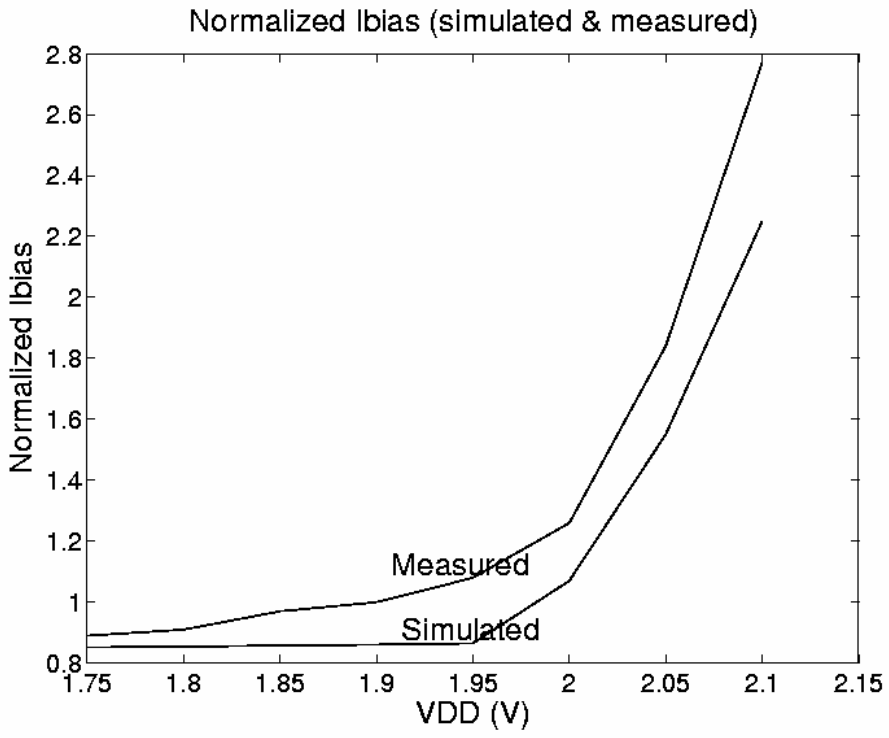


Figure 4.24. Variation of normalized I_{BIAS} with V_{DD} in the 0.25 μm CMOS process

In Figure 4.24, as the value of V_{DD} is decreased (in the range of 1.85 – 1.95 V), the value of I_{BIAS} remains fairly constant due to the forward-biased bulk drive of the PMOS transistors. As the value of V_{DD} is decreased further (in the range 1.75 – 1.85 V), there is a marginal decrease (maximum decrease is about 12%) in the value of I_{BIAS} as the forward biasing of the PMOS bulks are limited by the limiting current $I_{\lim}$ (set at 100 nA here) as shown in Figure 4.23. At this point, the bulk drive mechanism tends to approach its extreme limit. If the value of the limiting current $I_{\lim}$ is increased, then the value of I_{BIAS} will remain constant over a wider range for lower values of V_{DD}.

On the other hand, as the value of V_{DD} is increased (in the range 1.95 – 2.1 V), there is an increase in the value of I_{BIAS}. This can be explained by the fact that the bulks of the PMOS transistors are reversed biased to its maximum extent V_{DD}, and any increase in V_{DD} causes an increase in the value of V_{gs}, which in turn causes an almost exponential increase in I_{bias} (as the transistors are operated in weak inversion). The measured and the simulated data in Figure 4.24 for this biasing scheme corresponded closely to each other, which prove the viability of the biasing scheme.

An important point to note here is that *limited drive* of the bulks of the PMOS transistors can be done successfully in the CMOS process without experiencing latch-up problems. This mechanism of forward biasing the bulks, which helps in decreasing the threshold voltage, can be advantageous in generating appreciable bias currents for small power supply voltages.

Several different chips for the biasing circuit were tested, and the results are shown next.

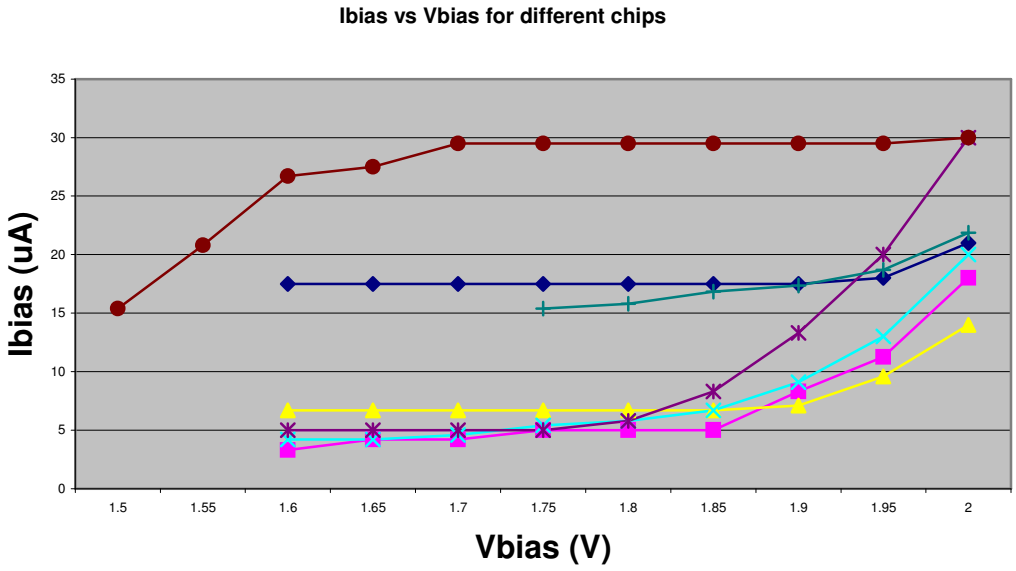


Figure 4.25. Variation of I_{BIAS} with V_{DD} in different chips in the 0.25 μm CMOS process

From Figure 4.25, it can be seen that there exists a wide variation in the bias current I_{BIAS} in different chips. The topmost curve in Figure 4.25 represents a case, which matches closely to the simulation as shown in Figure 4.24. In all these cases, the bulk drive of the PMOS transistors takes place successfully, and I_{BIAS} remains fairly constant over a particular range of V_{DD} for each of these chips. But, this value of I_{BIAS} (in the flat region) during the forward biasing of the PMOS bulks is different. Referring to Figure 4.23, this value of I_{BIAS} in the flat region is generated by comparing (equating) I_{BIAS} with the reference current in the

bootstrap circuit. If this reference current varies, it will be reflected on the value of I_{BIAS}. The following reasons can cause the variations in the reference current, generated in the bootstrap circuit:

1. Variations in the value of the resistor, R, in the bootstrap circuit will directly affect the reference current. Poly resistors were used during fabrication, and they could vary up to $\pm 30\,\%$ within the process.
2. In Figure 4.23, the offset voltage of the op amp, whose inputs are connected between the drains of M_{29} and M_{30}, can cause a major change in the reference current. This op amp is connected to keep the drains of M_{29} and M_{30} at the same potential as with minimum feature size devices, current mirroring is far from ideal. The voltage across the resistor R, V_R, can be given by

$$V_R = V_t \ln\left(\frac{A_2}{A_1}\right) \tag{4.35}$$

In presence of an offset voltage, V_{OS}, of the op amp, Equation (4.35) can be modified as

$$V_R = V_t \ln\left(\frac{A_2}{A_1}\right) \pm V_{OS} \tag{4.36}$$

Thus, the voltage across the resistor R will be affected by the input offset voltage of the op amp, and this will cause variations in the reference current. This op amp was designed as a two-stage op amp with current mirror load using all minimum feature size devices, which created an appreciable value for V_{OS}. This offset voltage was the major reason for wide reference current

variations in the Bootstrap circuit. This op amp should have been designed with longer channel length devices.

4.7.3 Measured Results of Op Amp *OP*2

Out of all the fabricated circuits, some of them were packaged, but most of them could not be packaged; they had to be wafer probed using a probe station. The measurement setup of the probe station is briefly discussed and is shown in Figure 4.26. In case of measurements involving packaged chips, the probe station in Figure 4.26 can be substituted by the packaged chip. A complete description of different equipment used in the testing is given in Table 4.14.

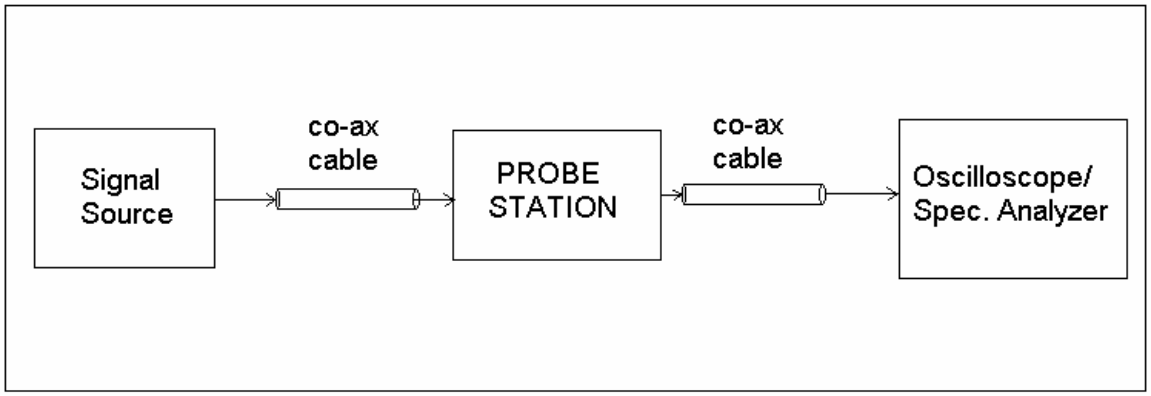


Figure 4.26. Measurement setup of the probe station

Table 4.14. Description of different equipments used during measurements

Purpose	**Part/Model Number**	**Comments**
To perform wafer-based probing	Micromanipulator Probe Station	This probe station was used to perform wafer-based probing. Mostly, low-frequency DC probes were used in probing. Co-axial cables were used to connect different probes to external equipments.
DC power supply	HP E3631A 0-6 V/ 5A	This power supply was used to provide DC voltages to the circuit.
Function generator	HP 33120A (15MHz) HP 8656B (5 Hz – 500 MHz)	These function generators were used to input sinusoidal and pulse waveforms to the circuit.
Multimeter	Keithley 2000 HP E2373A	These multimeters were used to measure DC voltages. Unfortunately, due to internal equipment faults, they were not able to measure DC currents, which had to be measured as a voltage drop across a resistor.
Oscilloscope	Tektronix TDS 460A (400 MHz)	It was used to observe the time-domain output waveforms.
Spectrum Analyzer	Rhode & Schwarz (20 Hz – 8 GHz)	It was used to observe the output frequency spectrum.
Network analyzer	HP 8751A (5 Hz – 500 MHz)	It was used to measure the small-signal gain and phase plots for the op amp.

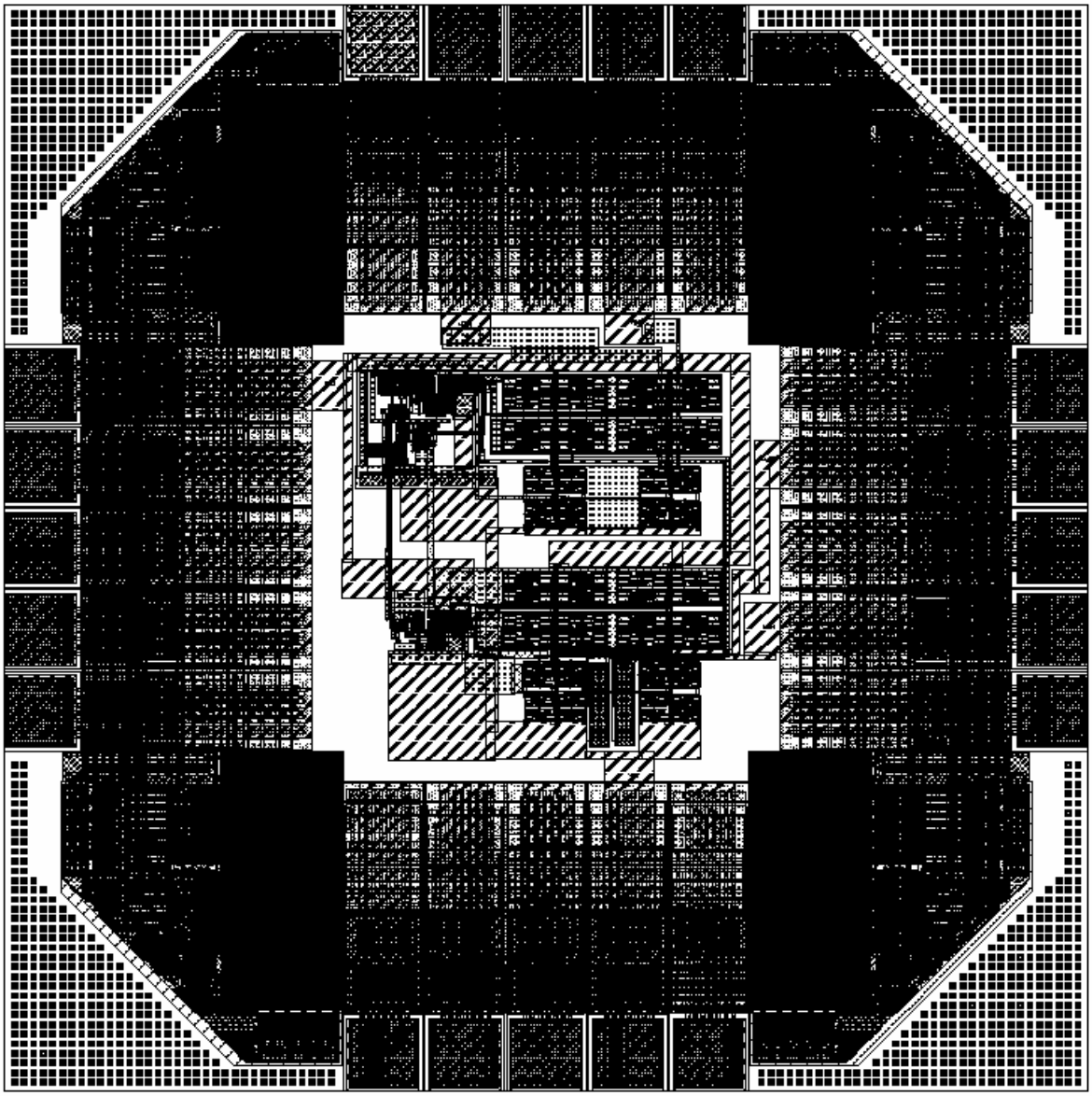


Figure 4.27. Layout of *OP2*

In Figure 4.27, the op map *OP2* is laid out in the center, and it is surrounded by the pads and ESD protection circuits.

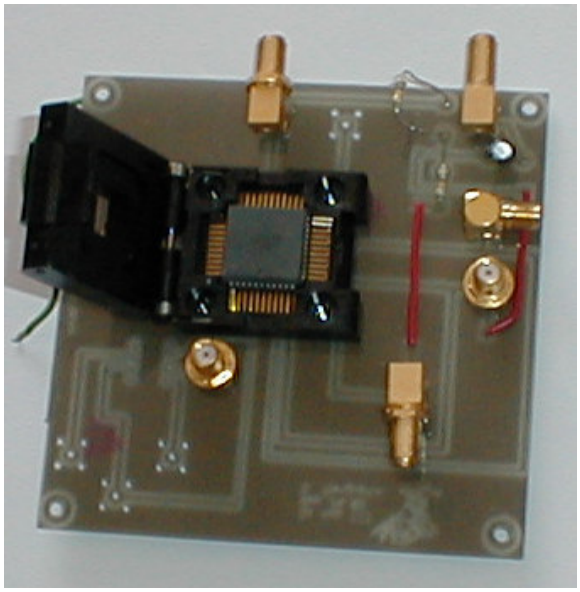


Figure 4.28. Photograph of the packaged *OP2* (PLCC 44 pin package) and the PCB

During wafer based measurements, the biggest limitation was in making high frequency measurements. As it can be seen in Figure 4.26, co-axial cables were used to connect the input/output devices to the probe station. These co-axial cables had large capacitances, which were in the order of 20 – 50 pF/foot. Their losses affected high frequency measurements. Another factor that degraded high-frequency measurements was the connection taps from the co-axial cable to the probe station; they also had significant losses at high frequencies. It was found that both of them together had a -3 dB bandwidth of about 15 MHz with reference to 50 Ω resistance.

The first performance specification of the op amp measured was its input offset voltage (V_{os}). The input offset voltage is caused by the mismatches in the devices during fabrication. These mismatches in a simple NMOS current mirror

sink were measured in Section 4.7.1, and an estimate of the input offset voltage for the op amp was developed in Equations (4.33) and (4.34).

In the 0.25 μm CMOS process, the nominal input offset voltage for this op amp was 4 mV. The variation of the input offset voltage with the input common-mode voltage in the 0.25 μm CMOS process is shown in Figure 4.29. The op amp was operated as a single-ended output unity-gain buffer configuration. The high-gain input common-mode range was 0.55 – 1.23 V**.** Outside this high-gain range, decrease in the value of the small-signal gain caused an increase in the input offset voltage.

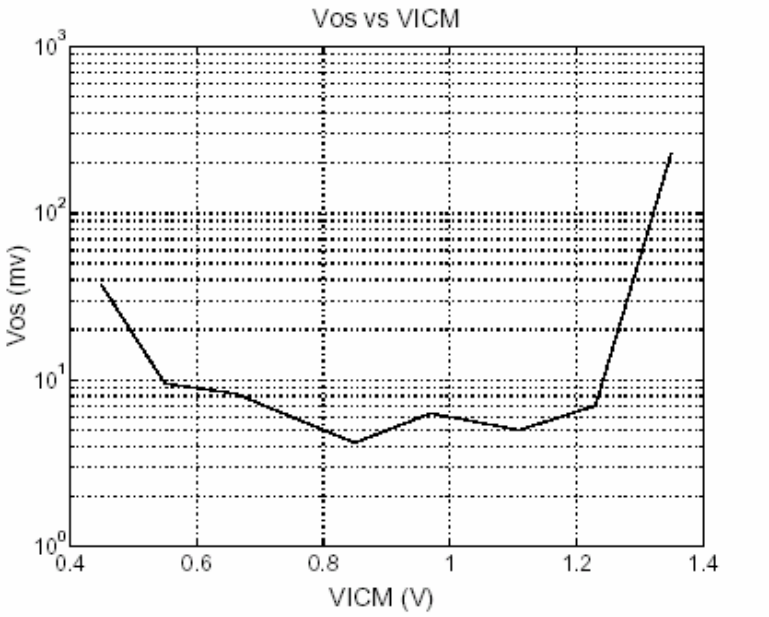


Figure 4.29. Variation of the input offset voltage with the input common-mode voltage in the 0.25 μm CMOS process

Referring to Figure 4.29, the input offset voltage remained fairly constant in the high gain input common-mode range. As the op amp was driven close to the

limits of the input common-mode range, its small-signal gain decreased. This caused an increase in the input offset voltage, which can be seen in the figure.

The input offset voltages of 14 samples were also measured in the 0.25 μm CMOS process. The input common-mode voltage in these measurements was set to 1 V. The minimum input offset voltage measured was 2.1 mV.

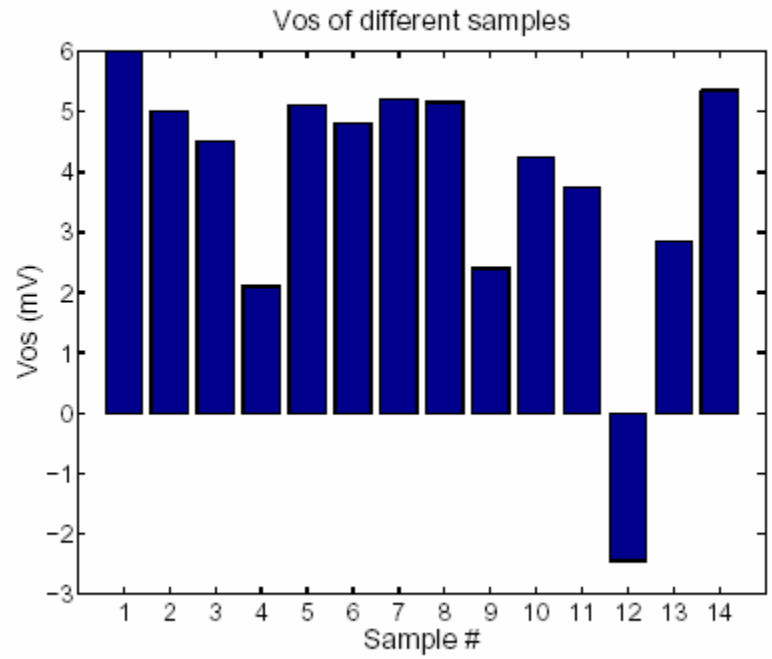


Figure 4.30. Input offset voltage of 14 chips in the 0.25 μm CMOS process

The variation of the input offset voltage was in the range of 2.1 – 6 mV. As shown earlier, there was a wide variation in the bias currents, but even with different bias currents, the op amps were able to function well with lower input offset voltages.

This op amp, OP2, was also fabricated in the 0.18 μm CMOS process. The circuit elements of this op amp were scaled from the 0.25 μm CMOS

process to the 0.18 μm CMOS process. The measured input offset voltage for OP2 in the 0.18 μm CMOS process is shown next in Figure 4.31.

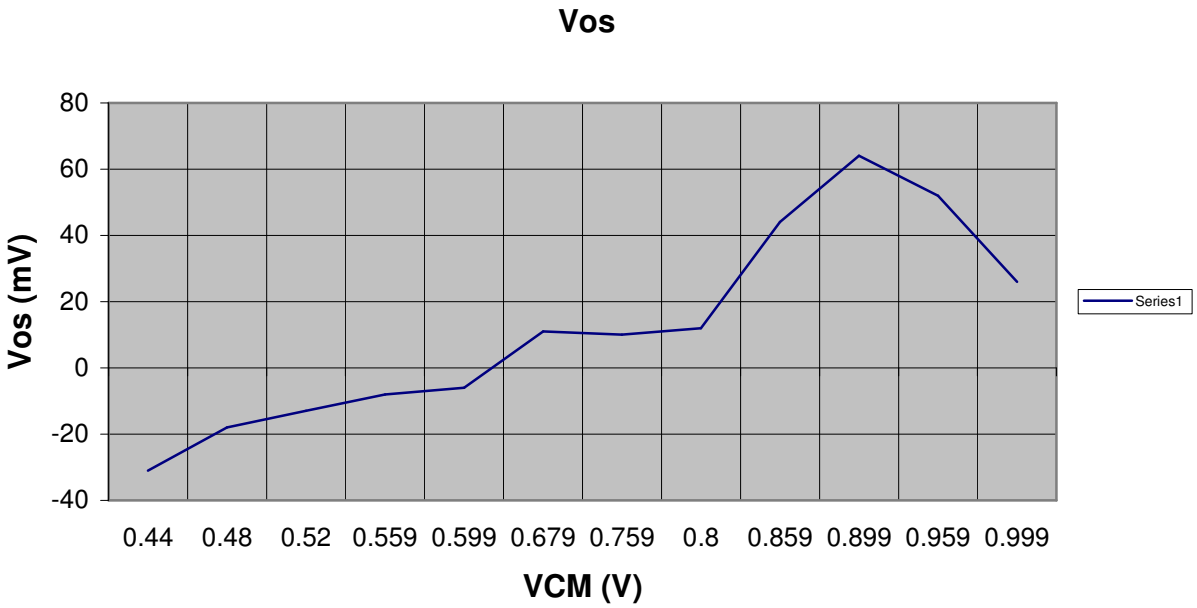


Figure 4.31. Variation of the input offset voltage with input common-mode voltage in the 0.18 μm CMOS process

From the above plot, it can be seen that the magnitude of the input offset voltage of this op amp is large, and it varies considerably across the input common-mode range. Measurements of the overall performance of the op amp is presented next.

4.7.4 Measurement results for *OP2* in the 0.25 μm CMOS process

The overall measured performance of *OP*2, connected as a single-ended output unity-gain buffer, in the 0.25 μm CMOS process is tabulated next in Table 4.15.

Table 4.15. Simulated and measured performance of *OP2* in the 0.25 μm CMOS process

SPECIFICATIONS	Simulated value	Measured value
Technology	0.25 μm CMOS	0.25 μm CMOS
Channel length (L)	0.25 μm	0.25 μm
VDD (V)	2	2
IDD (mA)	0.8	0.79
Maximum Vos (mV)	-	6
Av (dB)	71	56
UGBW	26 MHz (CL = 2 pF)	1 MHz (CL = 45 pF)
PM	60 deg (CL = 2 pF)	35 deg (CL = 45 pF)
SR	17 V/μs , -12 V/μs (CL = 2 pF)	3 V/μs (CL = 45 pF)
ICMR	0.46 – 1.4 V	0.41 – 1.567 V
PSRR (at dc)	Small signal: 73 dB	60 dB ($\Delta V_{DD} = 0.01$ V) 46 dB ($\Delta V_{DD} = 0.1$ V)
CMRR		-
Noise	6.2 μ V/$\sqrt{Hz}$ (1 Hz) 13 nV/$\sqrt{Hz}$ (400 KHz)	-

Table 4.15 summarizes the measured performance of the op amp *OP*2 in the 0.25 μm CMOS process with all 0.25 μm channel length devices. The value of A_v was only 56 dB. From simulation, this value was found to be 71 dB, but in reality, it was less than expected. Various factors could have attributed to this small value of A_v; one of them being the bulk drive of the PMOS devices. If the simulation models for the bulks of the PMOS devices are inaccurate, the simulation performance will be different from reality (the bulk simulation models could not be verified). Moreover, use of $L_{\min}$ based devices can lead to differences in the simulation and experimental results if the modeling of smaller channel lengths is not accurate. It is difficult to specifically determine the reasons, which resulted in poor small-signal gain of this op amp.

The measurements were made under different capacitive loading conditions at the output. During wafer probing, the output load capacitance was about 150 pF, and the packaged chip along with the PCB had an output loading capacitance of 45 pF. The output capacitance of the packaged chip and PCB was 45 pF, most of which was due to the large ESD diodes at the output pads and the PLCC package. While making wafer-based measurements, the output capacitance was 150 pF, which was primarily dominated by the high value of capacitances of the co-axial cables. These output loads were much larger than what this op amp was designed to drive. The large-signal slewing of the op amp was limited by the large output load capacitance. The comparison of the simulated and the measured performance under the same output loading conditions is tabulated in Table 4.16.

Table 4.16. Comparison of the simulated and measured performance of *OP2* in the 0.25 μm CMOS process under same output loading conditions

	CL = 150 pF (wafer probing)		CL = 45 pF (packaged chip)	
	Experimental	Simulated	Experimental	Simulated
UGBW (MHz)	1.1	2.75	6	10.2
PM (deg)	45	43	35	37
SR (V/us)	+1, -0.7	+1.4, -0.65	+3	+2.9, -2

Due to large capacitive loading, the phase margin was degraded, and the UGBW frequency was reduced. This op amp was designed to drive a maximum single-ended output capacitive load of 2 pF. But, while making measurements, the output capacitance was much larger than 2 pF. Although designed to drive a small output capacitance, this op amp was able to drive large output capacitances with reduced UGBW frequencies and acceptable phase margins.

With large output capacitances, the op amp did not oscillate, and it still had a positive phase margin. This happened because as the frequency increased, the capacitive reactance of the output capacitance decreased. This smaller capacitive reactance was in parallel with the large output resistance at the outputs of the op amp, which decreased the effective impedance at the outputs. This decrease in the output impedance caused a decrease in the value of small-signal gain, and it caused a faster roll-off of the gain with frequency resulting in a decreased UGBW frequency.

The op amp (*OP*2) made here was an un-buffered op amp. It is important to buffer the output internally in the chip so that huge external capacitive loadings can be driven by the output buffer stage. The buffered versions of this op amp are described in the following chapters. Some of the measurement plots for this un-buffered op amp are shown next.

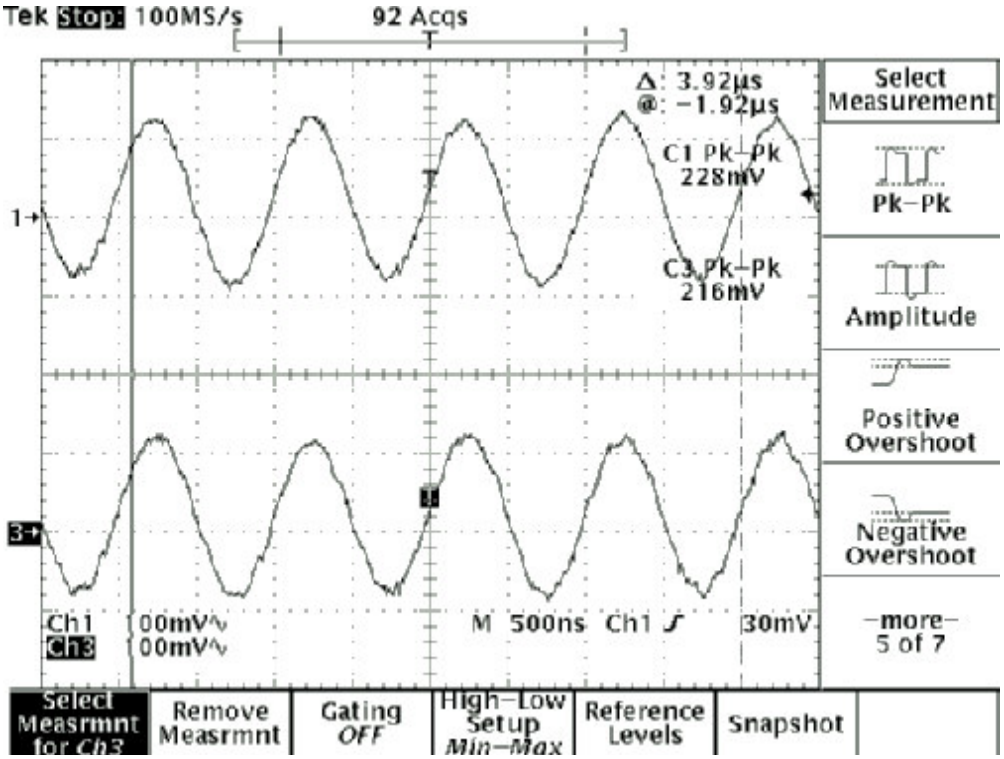


Figure 4.32. Input (Ch1) and output (Ch2) sinusoidal waveforms of *OP*2, connected as a unity-gain buffer, in the 0.25 μm CMOS process

The input and output waveforms were noisy due to large noise present in the wafer probing set up. This hampered the capability to make measurements with small amplitude signals.

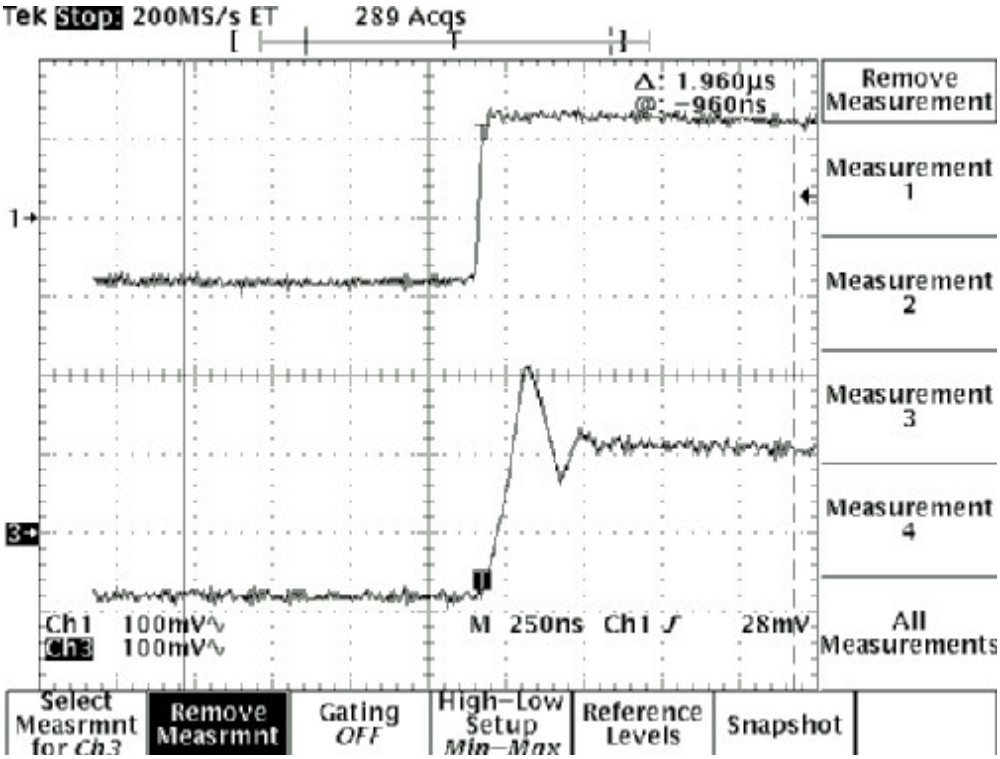


Figure 4.33. Input (Ch1) and output (Ch2) small-signal pulse waveforms of *OP*2, connected as a buffer, in the 0.25 μm CMOS process

In Figure 4.33, the top waveform is a 200 mV_{P-P}, 1 KHz pulse wave input to the buffer, and the output, with positive overshoot, is shown below it. The output capacitance was 45 pF. The positive overshoot can be observed in the output waveform as approximately 50%, which corresponds to an approximate phase margin of 35 degrees.

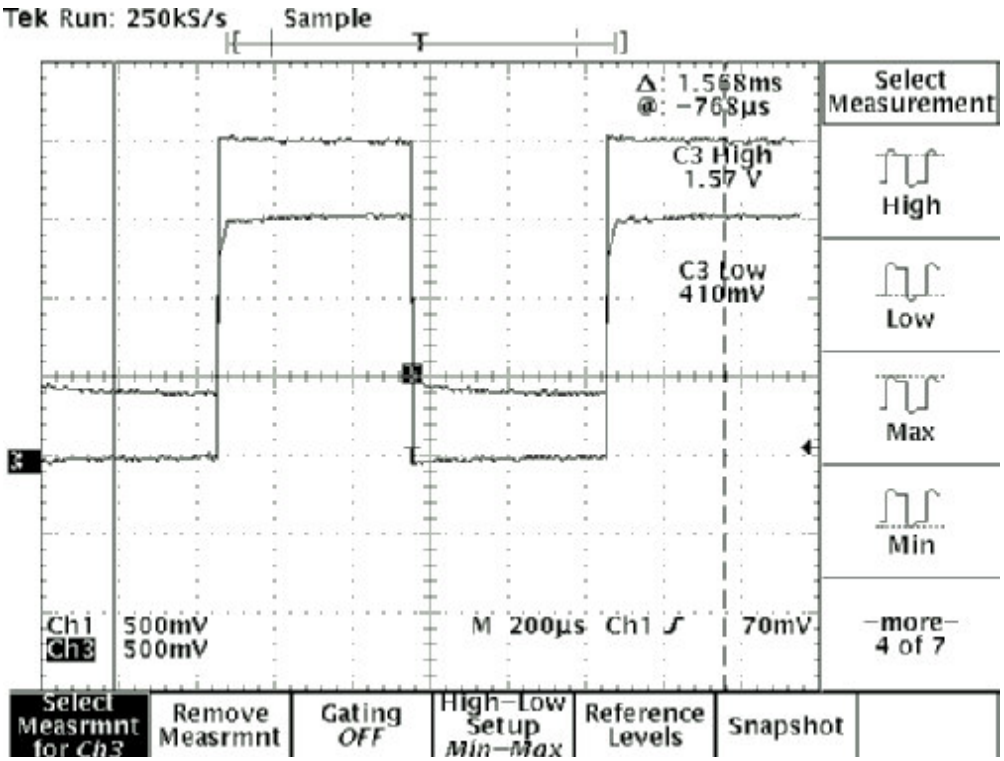


Figure 4.34. Large-signal input and output pulse waveforms of *OP*2, connected as a buffer, in the 0.25 μm CMOS process

The above plot shows the input and output waveforms under large signal condition. The applied input to the op amp, connected as a unity-gain buffer, was a 0 – 2 V pulse signal. The output saturated at the limits of the input-common-mode range (0.41 – 1.57 V).

This un-buffered op amp was designed to achieve a constant phase margin across different technologies. In the design, the phase margin was expressed as a ratio of bias currents in the two gain stages, which will remain constant. This suggests that the phase margin should also remain constant irrespective of the process variations within a particular technology. Within a technology, the bias currents might vary due to process variations, which will cause the UGBW to change. But, the phase margin should remain constant as long as the ratio of the bias currents of the two gain stages remains constant. As explained earlier in Chapter 3 (Figure 3.11), with proper functioning of the adaptive PMOS bulk drive mechanism; the bias currents in the two gain stages of *OP*2 are generated in such a way that their ratio will remain constant.

As it can be seen from measurements on the biasing circuit (Figure 4.25), wide variation in the reference current in the Bootstrap block can happen due to the offset voltage of the op amp in the Bootstrap block. A similar Bootstrap block was used to generate the limiting bulk-drive current, $I_{\lim}$, and it can also be expected to vary. Variation in this limiting current can cause variation in the maximum limit of threshold voltage modulation of the PMOS devices, thus affecting the bias current while the PMOS bulks are forward biased to their extreme limit. This will mainly affect the bias current in the second gain stage. Thus, the ratio of the bias currents in the two gain stages will be different, and it will affect the phase margin. Measurements on different packaged chips (CL = 45 pF) were made to verify process-independent phase margin in the 0.25 μm CMOS process, and they are shown in Table 4.17.

Table 4.17. Small-signal and transient performance of different chips in the 0.25 μm CMOS process

Chip #	Isupply (mA)	UGBW (MHz)	**PM (deg)**	SR (V/us)
1	0.72	6	**35**	3
2	0.71	5.5	**33**	3.34
3	0.65	5	**37**	2.24
4	0.53	5	**37**	1.25
5	0.48	3	**50**	1
6	0.35	5.5	**35**	3.04
7	0.35	4	**45**	2.36
8	0.3	4.2	**40**	2.04

In Table 4.17, the second column refers to the total supply current of the op amp, which is dependent on the biasing currents in the two gain stages. As seen from this table, due to the change in the biasing currents, both the UGBW and the slew rate were affected. But, the phase margin remained relatively constant for most of the chips.

4.7.5 Measurement results for *OP2* in the 0.18 μm CMOS process

The measured results for *OP*2 in the 0.18 μm CMOS process are presented in this section. The op amp was connected as a single-ended output unity-gain buffer. The first measurement made on this op amp was to check the gain when connected as a unity-gain buffer. The response is shown below in Figure 4.35.

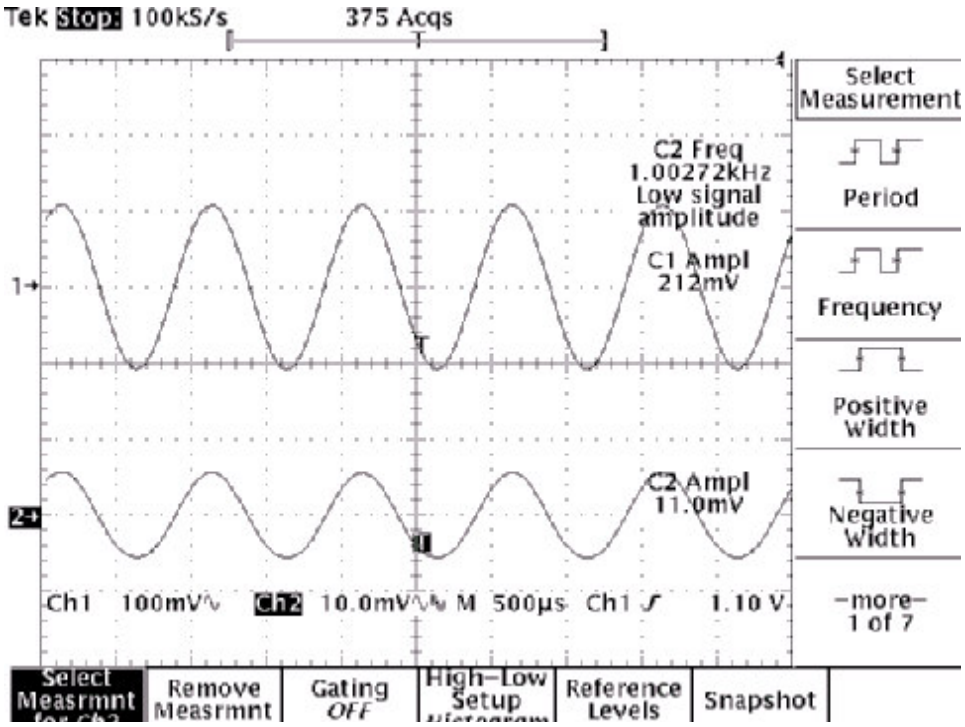


Figure 4.35. Input (Ch1) and output (Ch2) response of the op amp connected as a unity-gain buffer in the 0.18 μm CMOS process

In this measurement, the output waveform at the bottom has a 10X attenuation. It can be seen that the closed-loop gain is approximately 0.5 (expected value is 1). This suggests that the open-loop gain of the op amp is almost 1 (0 dB). The open-loop gain of this op amp was heavily degraded due to un-controlled bulk drive.

The supply current is shown in Table 4.18, which was about 3 times the simulated value. This suggests that the forward biasing of the PMOS bulk diodes were much larger than expected. The consequence of turning on of the PMOS bulks diodes is discussed next with the help of Figure 4.36.

Table 4.18. Measured performance of *OP*2 in the 0.18 μm CMOS process

Performance specification	Simulated value	Measured value
A_v	75 dB	0 dB
V_{os}	-	10 mV
I_{sup} $(V_{DD} = 1.5\ \text{V})$	0.75 mA	2.55 mA

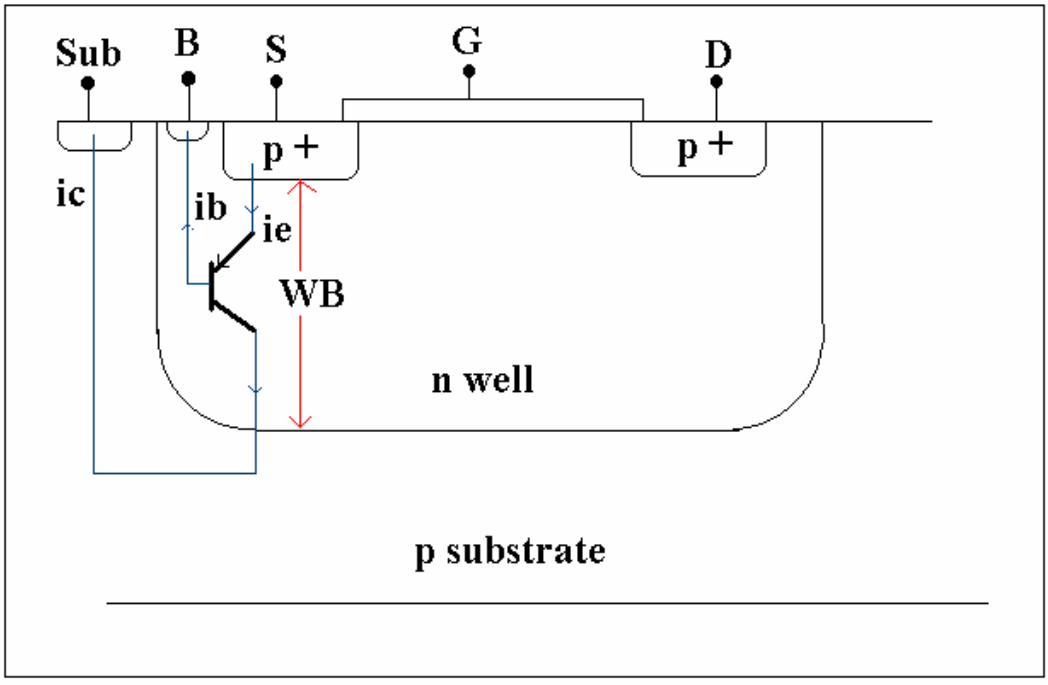


Figure 4.36. Parasitic p-n-p bipolar transistor associated with the PMOS device in an n-well CMOS process

Every PMOS device, made in an n-well, has a parasitic p-n-p bipolar transistor associated with it. In Figure 4.36, the bulk current of the PMOS device represents the base current of the p-n-p device. So, in *OP1* and *OP2,* controlling the bulk current refers to controlling the base current of the p-n-p device. The only important aspect relevant to the design of the gain stages is that the transconductance of the forward-biased p-n diode formed at the source of the PMOS device should be low, such that it does not cause the source of the PMOS device to become a low impedance node. Due to large emitter current, if the source of the PMOS device does become a low impedance node, then referring to Figures 3.9 and 3.10, the impedance at the sources of M9 and M10 will be dependent on the transconductance of the forward-biased p-n diodes. This will generate a negative resistance which will no longer be dependent on the g_{ds} terms, but will depend mostly on the g_m of the forward-biased bulk diodes. Consequently, this will result in an effectively negative differential output resistance of the gain stages, and it will also cause a drastic decrease in the magnitude of the differential gain.

The operation on the parasitic p-n-p device is strongly dependent on the depth of the "n well", which forms the base width (WB) of the bipolar device. In general, the collector-to-base current gain, which is given by β, is inversely proportional to WB; the smaller the base width, higher is the β.

If WB is large enough such that β is negligible, then all the current flowing into the emitter (source) goes out of the base (n-well), and negligible current will flow as the collector current through the p-substrate. In this case, the

bulk drive current will be almost equal to the current through the source terminal of the PMOS device.

On the other hand, if WB is small such that β has an appreciable value, then the current flowing through the emitter (source) will be (β+1) times the bulk drive current. In this case, even though one can choose a small magnitude of the bulk drive current, the current through the forward-biased p-n diode can be much larger, which will make the source of the PMOS device a low impedance node. Thus, the depth of the n-well plays a crucial role in order to have successful bulk drive. In this design, the bulk drive scheme worked well in the 0.25 μm CMOS process, but it failed in the 0.18 μm CMOS process. This happened because the depth of the n-well was less in the later. The forward biased PMOS bulk diodes caused low impedance nodes at the differential outputs, which resulted in very poor small-signal gain of the op amp in the 0.18 μm CMOS process. Overall, the adaptive PMOS bulk-drive scheme failed in this process.

4.8 Summary of $L_{\min}$ -based Design

In the chapter, the compensation of the overall two-stage op amp was discussed. The op amp consisted of two identical, cascaded gain stages, which were developed in the previous chapter. The phase margin of the op amp was expressed as a ratio of transconductances/currents, which ensured a relatively constant phase margin for different channel lengths and technologies. Other op

amp performance specifications, like ICMR, PSRR, noise were also discussed in this chapter.

The comparison of the performance of L_{min}-based op amp in two different CMOS processes was presented. This op amp was designed to achieve high gain and constant phase margin, independent of device channel length and technology. A study of the matching of the device geometries for L_{min}-based devices was carried out, and it showed poor matching for small channel lengths. This directly affected the performance (specially input offset voltage) of the op amps. Even though the simulated value of the small-signal gain was good, its measured value was poor with all L_{min}-based devices. Poor modeling of the small channel devices could have caused this discrepency between the simulated and measured gain. It could also have been caused by inaccurate modeling of the bulks of the PMOS devices. The adaptive PMOS bulk drive scheme worked well in the 0.25 μm CMOS process, but it failed in the 0.18 μm CMOS process because of excessive forward biasing of the source-to-bulk diodes. This failure of the biasing scheme did not result in a good op amp. Through simulations, the noise in the 0.18 μm CMOS process was observed to be less than the noise in the 0.25 μm CMOS process. It can be concluded that using the minimum feature-size channel length is not advantageous; it has more problems than its merits. But, the concept of the scalable architecture, where the phase margin can be expressed as a ratio, can be successfully extended into different technologies.

In the next chapter, a third topology of op amps (referred to as *OP3*) are presented. They are built using devices, which have twice the minimum feature-

size channel lengths, and the bulk-drive scheme is eliminated. They are designed to achieve large gain and constant UGBW and phase margin across technologies and channel lengths.

Chapter 5

Technology-Independent Op Amp Design with Constant Gain Bandwidth and Phase Margin

In the previous chapter, the design of an op amp (*OP*2) with technology-independent phase margin was presented. The phase margin was expressed as a ratio of bias currents, and the same architecture, when fabricated in different CMOS processes, was designed to have the same phase margin. This op amp used a negative resistance scheme to achieve large small-signal gain. The measured performance of *OP*2 in two different CMOS processes was discussed in the previous chapter.

The unity gain-bandwidth frequency (UGBW) of an op amp is an important performance specification, and *OP*2 could not achieve constant bandwidth. The UGBW of the two-stage op amp can be given by

$$UGBW = \frac{g_{mI}}{C_C} \tag{5.1}$$

where, g_{mI} represents the input transconductance of the first gain stage, and C_C is the value of the compensation capacitor. As it can be seen, the UGBW frequency is dependent on the transconductance, which is technology dependent. Thus, *OP*2 did not have a constant UGBW frequency. In this chapter, the design of an op amp (referred to as *OP*3) with constant UGBW and phase margin is explained. *OP*3 will achieve a constant UGBW due to a constant g_m, which will be shown to be independent of the *technology-dependent* parameters.

The design of *OP*2 was done using all minimum feature-size transistors. It also used the forward-biased bulk drive of the PMOS transistors to achieve the desired ratio of the bias currents in the two gain stages. From the measured results, it was found that the use of minimum feature-size lengths has more disadvantages than advantages, and the circuit performance is greatly degraded. In the design of *OP*3, the following modifications are made:

- Small channel lengths are used, but they are kept larger (about twice) than the minimum feature-size channel length in the technology.
- Bulk drive of the PMOS transistors is avoided, and all the PMOS and the NMOS bulks are reversed biased.
- The Miller compensation scheme is also modified to have better phase margin with less power.

5.1 Generation of Technology-Independent g_m

The UGBW of the op amp is dependent on g_m of the input transistors. In order to achieve a technology-independent UGBW, the value of g_m should be made independent of technology. Different circuit techniques for generating constant transconductance can be found in [45, 46]. The transconductance of a MOSFET in strong inversion can be expressed as

$$g_m = \sqrt{2K'\left(\frac{W}{L}\right)I} \tag{5.2}$$

where, K' is a *technology-dependent* parameter, and it varies with technology.

The transconductance of the MOSFET in weak inversion is given by

$$g_m = \frac{I}{nV_t} \tag{5.3}$$

where, n is dependent on technology. From Equations (5.2) and (5.3), it can be seen that even though the bias current through the MOS device can be kept constant using a bootstrap circuit, the transconductance will still vary due to its dependence on the *technology-dependent* parameter. A bootstrap circuit with BJTs, which can achieve a constant g_m, is described next in Figure 5.1.

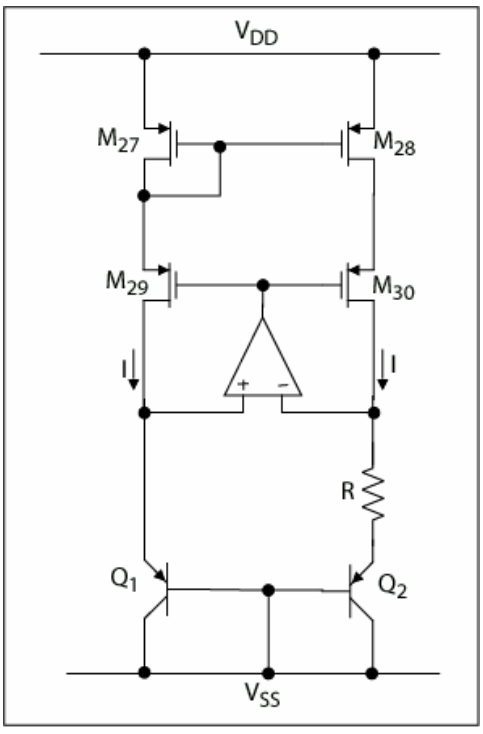


Figure 5.1. Bootstrap circuit with BJTs

Referring to Figure 5.1, the bipolar p-n-p transistors are the substrate BJTs available in the CMOS technology. It is important to note that in most of the

CMOS processes, these substrate p-n-p devices are the only bipolar transistors available in that process. The magnitude of the generated reference current (I) can be given by

$$I = \frac{V_t \ln\left(\frac{A_{Q2}}{A_{Q1}}\right)}{R} \tag{5.4}$$

And, the transconductance of Q_1 is given by

$$g_{m,Q1} = \frac{I}{V_t} = \frac{\ln\left(\frac{A_{Q2}}{A_{Q1}}\right)}{R} \tag{5.5}$$

Neglecting the variations in R during fabrication, the transconductance given by Equation (5.5) is independent of the technology, and it can be generated as a constant transconductance across different technologies. If the reference current, I, was mirrored into the differential input transistors of a BJT op amp, then the transconductance of the input bipolar transistors will be the same as Q_1, which will yield a constant UGBW. But, the op amps presented in the previous chapters have NMOS input stage. Let us consider the case where NMOS devices replace the BJTs in Figure 5.1 such that a constant NMOS transconductance can be generated [1]. It is shown next in Figure 5.2.

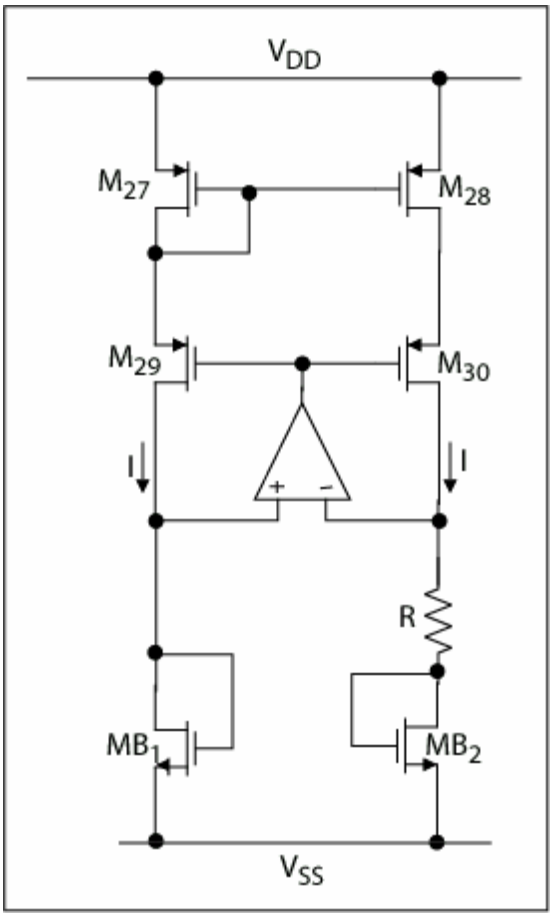


Figure 5.2. Bootstrap circuit with MOSFETs

In Figure 5.2, let us consider the case when the MOSFETs MB_1 and MB_2 are operated in weak inversion. Their drain current and transconductance are given by

$$I = \frac{nV_t \ln\left(\frac{W_{B2}}{W_{B1}}\right)}{R} \tag{5.6}$$

$$g_{m,B1} = \frac{I}{nV_t} = \frac{\ln\left(\frac{W_{B2}}{W_{B1}}\right)}{R} \tag{5.7}$$

From Equation (5.6), it can be seen that across different technologies, the drain current will vary due to variations in n, but the transconductance of the transistor MB_1 will remain constant across them (neglecting the variations in R during fabrication). If the MOSFETs, MB_1 and MB_2, are operated in strong inversion, the drain current and transconductance are given by

$$I = \frac{2}{K' R^2 \left(\frac{W}{L}\right)_{B1}} \left[1 - \sqrt{\frac{W_{B1}}{W_{B2}}}\right]^2 \tag{5.8}$$

$$g_{m,B1} = \sqrt{2K' \left(\frac{W}{L}\right)_{B1} I} = \frac{2}{R}\left[1 - \sqrt{\frac{W_{B1}}{W_{B2}}}\right] \tag{5.9}$$

Again, in strong inversion, the drain current will vary due to variations in K', but the transconductance will remain constant across different technologies (neglecting the variations in R during fabrication). If the size of the differential input transistors of the op amp are same as MB_1, and the same current, I, is mirrored into them, then the input transconductance of the op amp will remain constant, resulting in a constant UGBW frequency. The variation in the value of the resistor, R, can be large due to process variations, which will affect the value of g_m and consequently the UGBW. This resistor can be made more accurate through different layout techniques, and it can also be trimmed after fabrication. Shown next in Table 5.1 is a comparison of the currents and the transconductances that can be generated using the Bootstrap technique.

Table 5.1. Comparison of the drain current and the transconductance generated using the bootstrap circuit

	BJT	MOS (weak inversion)	MOS (strong inversion)
I	$\frac{V_t \ln\left(\frac{A_{Q2}}{A_{Q1}}\right)}{R}$	$\frac{nV_t \ln\left(\frac{W_{B2}}{W_{B1}}\right)}{R}$	$\frac{2}{K' R^2 \left(\frac{W}{L}\right)_{B1}}\left[1-\sqrt{\frac{W_{B1}}{W_{B2}}}\right]^2$
g_m	$\frac{\ln\left(\frac{A_{Q2}}{A_{Q1}}\right)}{R}$	$\frac{\ln\left(\frac{W_{B2}}{W_{B1}}\right)}{R}$	$\frac{2}{R}\left[1-\sqrt{\frac{W_{B1}}{W_{B2}}}\right]$

In Table 5.1, it can be seen that while moving across different technologies, the reference current will vary in the Bootstrap circuit implemented using the diode-connected NMOS loads (as shown in Figure 5.2), but their transconductance can be made relatively constant. Thus, in different technologies, the reference current will change in order to generate a constant NMOS transconductance. This Bootstrap circuit (Figure 5.2) will not generate a constant reference current, but it will generate a constant NMOS transconductance across different technologies. The development of the gain stage of *OP*3 is discussed in the next section. This op amp will be designed to achieve constant UGBW frequency and phase margin across different technologies.

5.2 Gain Stage of *OP*3

The gain stage of *OP*3 is identical to the gain stage of *OP*2, but it has a simpler biasing circuit, which is shown in Figure 5.3. The bulks of both the PMOS and the NMOS transistors are always kept reversed biased. Moreover, the use of minimum feature-size channel length is avoided in this design. The channel lengths are kept small, but they are made larger (almost twice) than the minimum feature-sizes in the technology. For example, in the 0.25 μm CMOS technology, the channel length used was 0.55 μm, and in the 0.18 μm CMOS technology, the channel length used was 0.35 μm. This way, during the fabrication process, the limits of the lithography process are not pushed, and better matching can be achieved. The transistors in this design are operated in strong inversion.

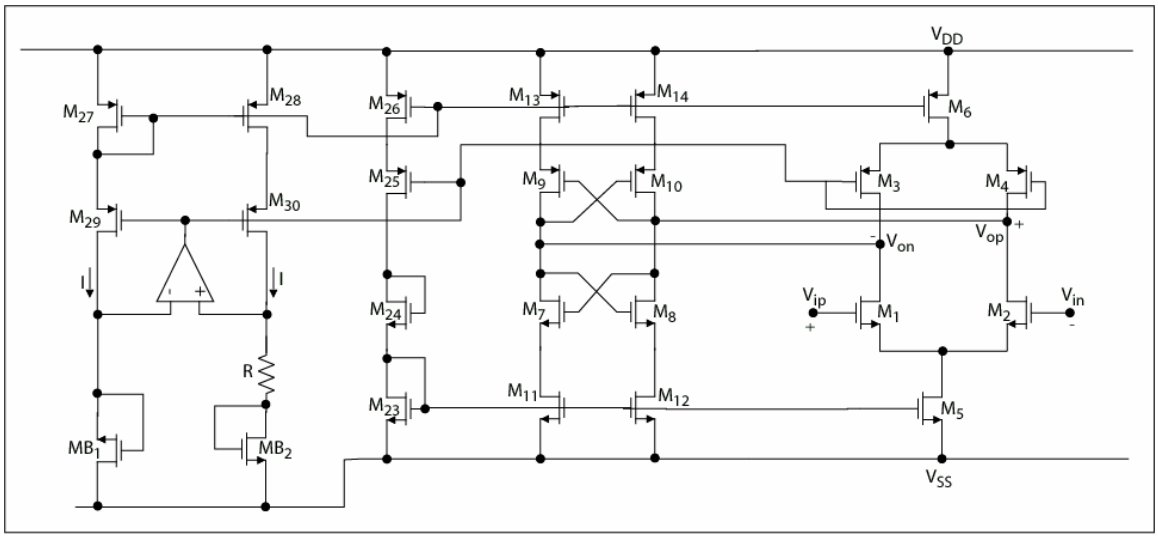


Figure 5.3. Gain stage of *OP*3

Table 5.2. Aspect ratios of transistors in the gain stage of *OP3*

$S_1 = S_2 = 0.5S_5 = S_7 = S_8 = S_{11} = S_{12} = S_{23} = S_{24}$	100X
$S_3 = S_4 = 0.5S_6 = S_9 = S_{10} = S_{13} = S_{14} = S_{25} = S_{26} = S_{27} = S_{28} = S_{29} = S_{30}$	200X
$S_{B2} = 2S_{B1}$	200X
R	720 Ω

$* S_i = \left(\frac{W}{L}\right)_i$

Referring to Figure 5.3, the magnitude of the reference current, I, in the bootstrap stage can be given by Equation (5.8). The same current is mirrored into the input transistors M_1 and M_2. So, from Equation (5.9), the input transconductance can be given by

$$g_{m1} = \frac{2}{R}\left[1 - \sqrt{\frac{W_{B1}}{W_{B2}}}\right] = \frac{0.6}{R} = 0.814 \text{ mS} \qquad (5.10)$$

In reality, the input transconductance will be slightly less than the value given by Equation (5.10) because it represents the transconductance of MB_1, which does not suffer from bulk effect. Though the same current is carried by both MB_1 and M_1, M_1 will suffer from bulk effect, which will tend to slightly decrease the transconductance of M_1 as compared to MB_1.

5.3 Compensation of *OP*3

The overall op amp, *OP*3, is a two-stage op amp as shown below in Figure 5.4. It has two cascaded gain stages, G_1 and G_2, where each gain stage has the same architecture as shown in Figure 5.3. The only difference in these two gain stages is in the aspect ratios of the transistors. The aspect ratio of all the transistors in G_2 was made twice of that of G_1 (shown in Table 5.2), i.e., G_2 is a 2X scaled version of G_1. Thus, the bias current in G_2 is twice as that in G_1. Referring to the design of the op amps *OP*1 and *OP*2, for good phase margin, the ratio of the bias currents in the two gain stages was made as 5. In the design of *OP*3, this ratio of the bias currents in the two gain stages is made 2, which is easier to implement.

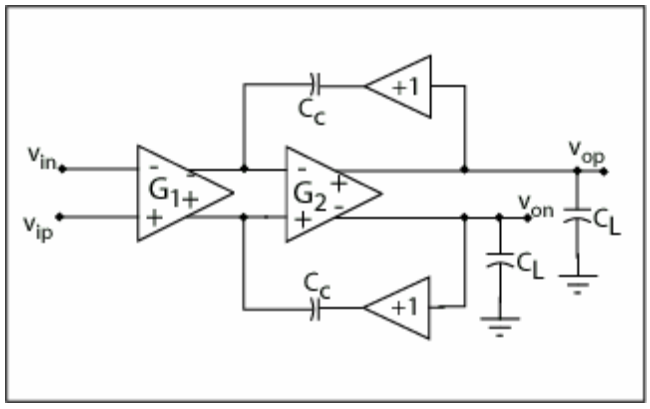


Figure 5.4. Compensation of *OP*3

The compensation of *OP*3 is similar to the compensation of *OP*2, but additional buffers are added in the Miller compensation paths to improve the phase margin by eliminating the RHP zeros caused by the compensation capacitors. These

buffers were implemented in transistor level using simple NMOS and PMOS source followers as shown in Figure 5.5.

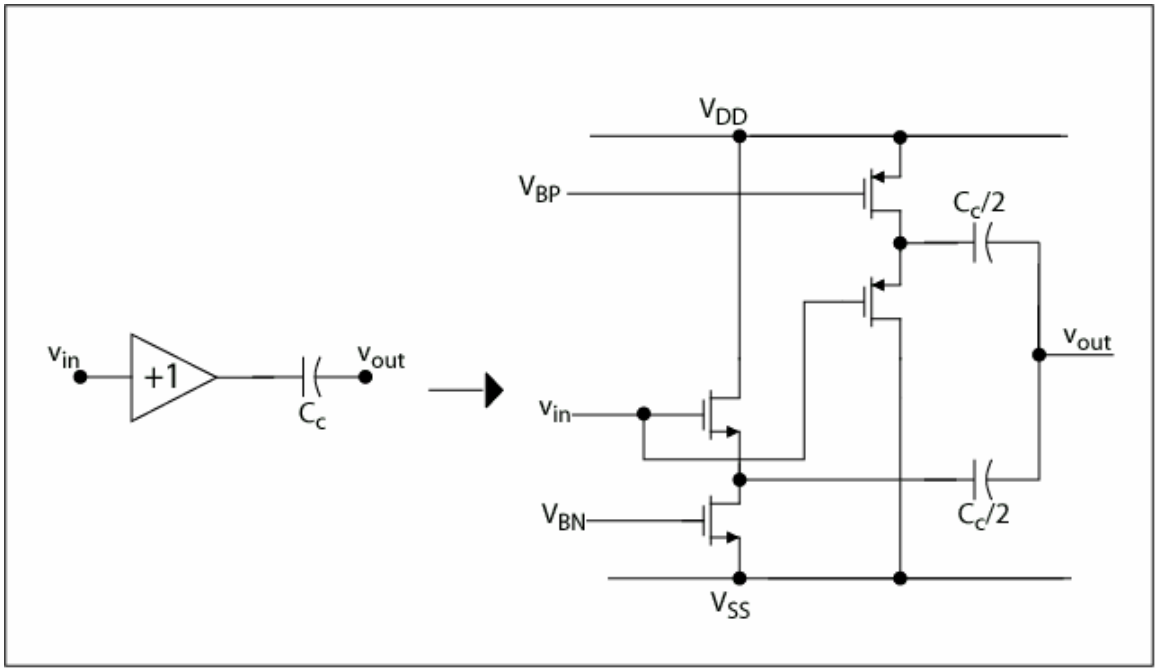


Figure 5.5. Transistor-level implementation of the unity-gain buffers in *OP3*

Figure 5.5 shows the implementation of the buffers in the Miller feedback path. Each buffer is implemented using a combination of NMOS and PMOS source followers. Referring to Figure 5.4, to understand the compensation scheme, let,

g_{m1} = transconductance of the first gain stage (G_1).

R_1 = load impedance to ac ground seen at each of the output nodes of G_1.

g_{m2} = transconductance of the second gain stage (G_2).

R_2 = load impedance to ac ground seen at each of the output nodes of G_2.

$C_{L,\max}$ = maximum external single-ended load capacitance to be driven.

A_{V1}, A_{V2} = gains of G_1 and G_2 respectively.

Considering a differential-input, differential output configuration, the UGBW can be given by

$$UGBW = \frac{g_{m1}}{C_C} \tag{5.11}$$

Substituting Equation (5.10) in (5.11), we get

$$UGBW = \frac{2}{RC_C}\left[1 - \sqrt{\frac{W_{B1}}{W_{B2}}}\right] \tag{5.12}$$

Similarly, for a differential-input, single-ended output configuration, the gain bandwidth can be given by

$$UGBW = \frac{g_{m1}/2}{C_C} \tag{5.13}$$

$$UGBW = \frac{1}{RC_C}\left[1 - \sqrt{\frac{W_{B1}}{W_{B2}}}\right] \tag{5.14}$$

As it can be seen from Equations (5.12) and (5.14), neglecting the variation in the passive components (R, C) during fabrication, the gain bandwidth can be made constant. The calculation of the phase margin for differential-in, single-ended out configuration is presented next. It is derived for a single-ended output configuration of the op amp.

$$A_{V1} = g_{m1}R_1 \quad \text{and} \quad A_{V2} = g_{m2}R_2 \tag{5.15}$$

The overall gain, for single-ended output configuration, is given by

$$A_V = A_{V1}\left(\frac{A_{V2}}{2}\right) \tag{5.16}$$

The dominant pole (at the outputs of G_1) is given by

$$p_1 = \frac{-1}{R_1(A_{V2}C_C)} \tag{5.17}$$

The load pole (at the outputs of G_2) is given by

$$p_L = \frac{-g_{m2}}{C_{L,\max}} \tag{5.18}$$

The UGBW frequency, while operating the op amp in single-ended output configuration, is given by

$$UGBW = \frac{A_V}{2} p_1 = \frac{g_{m1}}{2C_C} \tag{5.19}$$

The ratio of UGBW to the load pole is given by

$$\frac{UGBW}{p_L} = \left(\frac{g_{m1}}{g_{m2}}\right)\left(\frac{C_{L,\max}}{2C_C}\right) \tag{5.20}$$

Let us choose the value of the internal miller compensation capacitor to be

$$C_C = C_{L,\max} \tag{5.21}$$

For the aspect ratios of the transistors in the two gain stages, we have

$$g_{m2} = 2g_{m1} \tag{5.22}$$

Now, we can modify Equation (5.20) as

$$\frac{GBW}{p_L} = \frac{1}{4} \tag{5.23}$$

The RHP zero caused by C_C is eliminated by the unity-gain buffers in the Miller feedback path. These unity-gain buffers also help in improving the phase margin by introducing a pole-zero pair at the op amp output. Considering a feedback system, any pole in the feedback path always appears as a zero at the overall

output. The pole at the output of these unity-gain buffers in the Miller compensation paths (which are in the feedback path) appears as a LHP zero at the overall op amp output, and they can be given by

$$z_1 = \frac{-g_{m,buffer}}{C_C/2} \tag{5.24}$$

In this design, with proper scaling of the currents and widths of the transistors in these unity-gain buffers, the value of $g_{m,buffer}$ was chosen as

$$g_{m,buffer} = \frac{g_{m1}}{2} \tag{5.25}$$

Thus, the ratio of the UGBW frequency and the LHP zero will be

$$\frac{UGBW}{z_1} = \frac{1}{2} \tag{5.26}$$

These unity-gain buffers will also introduce a pole at the op amp outputs. This pole is greater but very close to the zero caused by the buffer. So, the effect of the pole-zero pair introduced by the buffers at the op amp output is negligible; it only has marginal affects on the gain and the phase responses.

Neglecting other higher order poles and zeros, the transfer function of this op amp can be approximated by a two-pole system; both the poles being given by Equations (5.17) and (5.18). Thus, from Equation (5.23), the phase margin will be 76°. When the value of C_C is set of 1 pF (for a maximum load capacitance of 1 pF), then from Equation (5.14), it should achieve an approximate UGBW of 66 MHz. The zero caused by the buffers can slightly affect the UGBW and the phase margin. Other performance specifications of *OP3* are similar to *OP2*, which were discussed in Chapter 4.

5.4 Simulation Results

In the previous sections, the design of *OP*3 with constant UGBW frequency and phase margin was presented. The simulation results for this op amp in the 0.25 μm CMOS and the 0.18 μm CMOS processes are presented in this section.

5.4.1 Simulation Results of *OP*3 in the 0.25 μm CMOS Process

The simulated performance of *OP*3, as a unity-gain buffer, in the 0.25 μm CMOS process (with all 0.55 μm channel length devices) is shown in Table 5.3.

Table 5.3. Simulated performance of *OP*3 in the 0.25 μm CMOS process

Performance specification	**Simulated value**
A_v	98 dB
UGBW (single-ended CL= 1 pF)	60 MHz
Phase margin	92 deg
Slew rate (single-ended CL= 1 pF)	+60, -50 $V / \mu s$
ICMR (Vdd = 2 V)	0.62 – 1.46 V
CMRR	90 dB
PSRR	92 dB
Input referred noise	9.5 $\mu V / \sqrt{Hz}$ (1 Hz) 14.5 $nV / \sqrt{Hz}$ (2 MHz: corner frequency)
Idd	960 μA

The simulation plots for this op amp in the 0.25 μm CMOS process with all 0.55 μm channel length devices are shown next. The op amp was connected in a single-ended, unity-gain configuration.

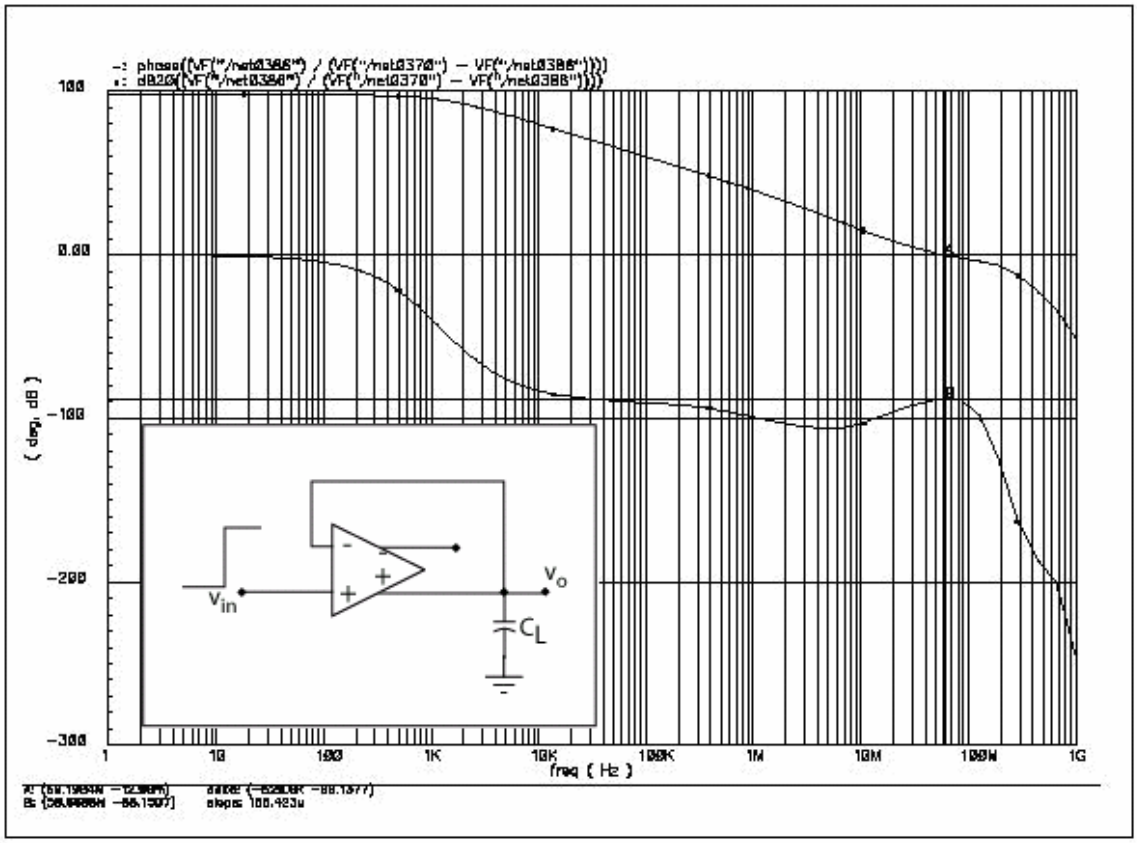


Figure 5.6. Small-signal simulation results of *OP*3 (single ended) in the 0.25 μm CMOS process

(Y axis: Magnitude in dB, Phase in degrees; X axis: Frequency in Hz)

A_v = 98 dB

UGBW (single-ended CL = 1 pF) = 60 MHz

PM = 92 deg

It can be seen that while using twice the channel length compared to the ones in *OP*1 and *OP*2, one can achieve very large value of the small-signal gain with the help of the negative resistance scheme.

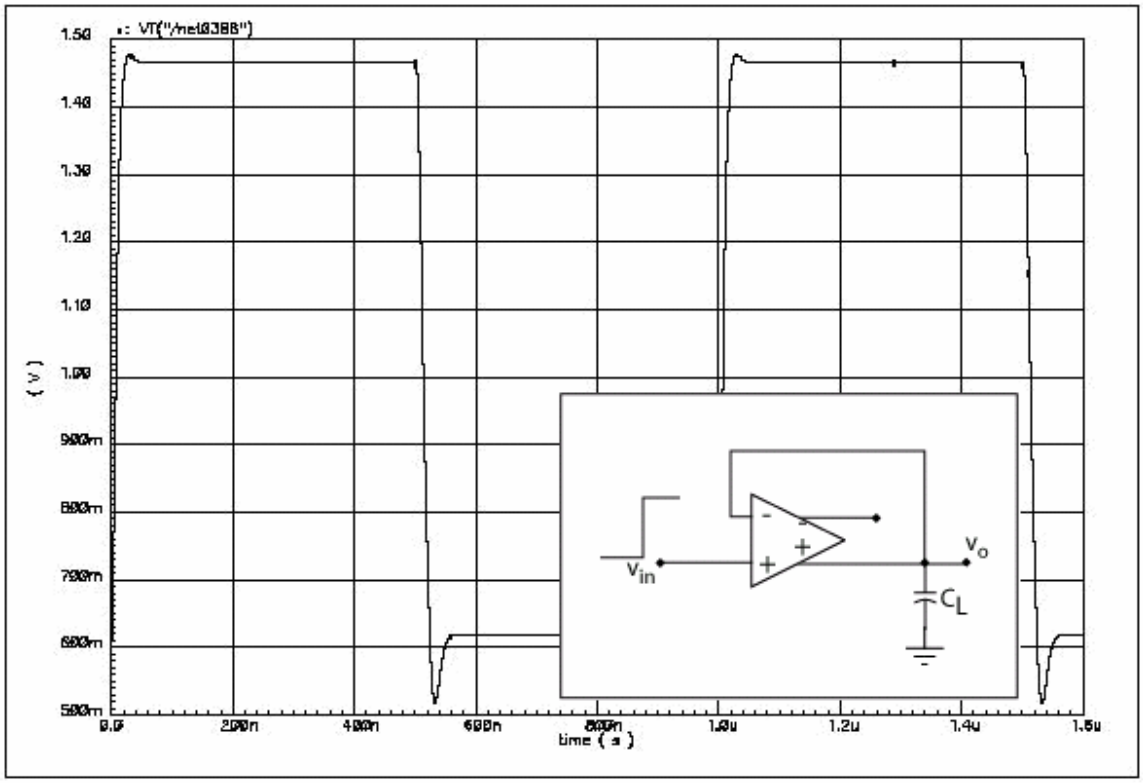


Figure 5.7. Slew rate of *OP*3 connected as a buffer with single-ended load capacitance of 1 pF in the 0.25 μm CMOS process

(Y axes: Output in Volt; X axes: time)

$$SR^{+} = +60 \;\; V / \mu s$$

$$SR^{-} = -50 \;\; V / \mu s$$

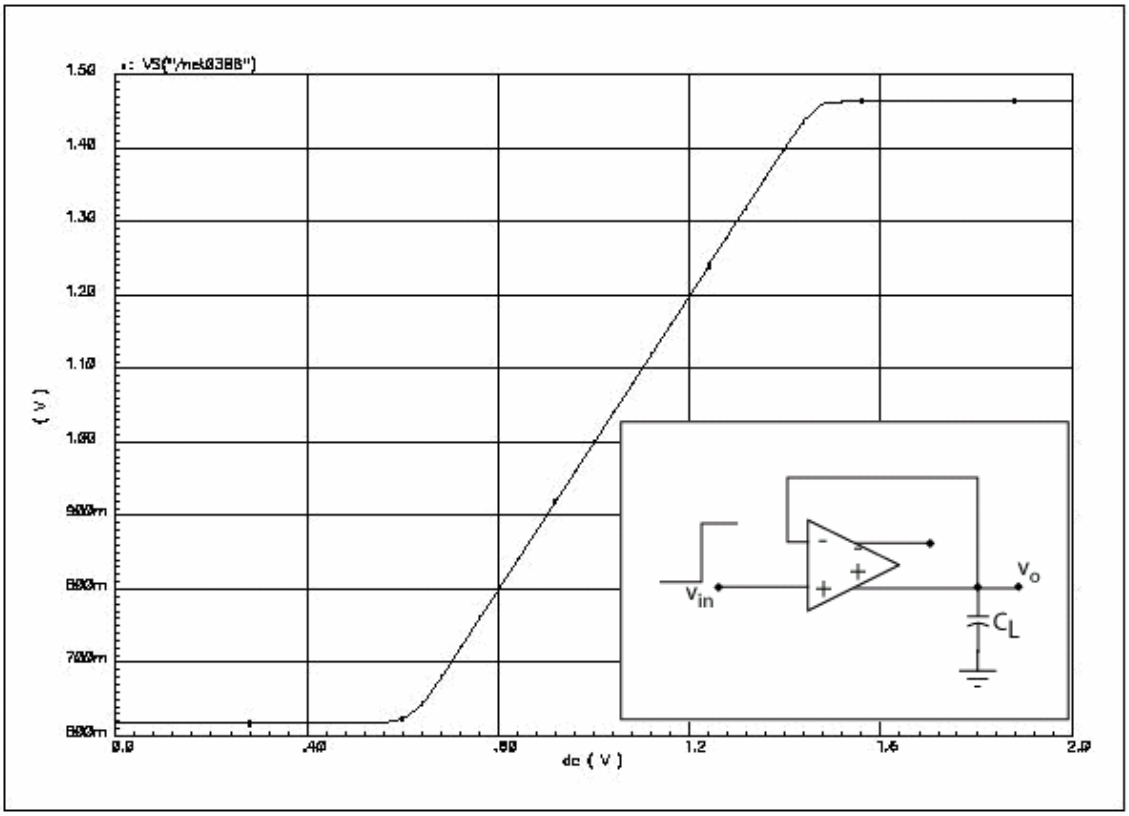


Figure 5.8. Input common-mode range of *OP*3 connected as a buffer in the 0.25 μm CMOS process

(Y axis: Output in Volt; X axis: Input in Volt)

ICMR = 0.62 – 1.46 V

Vdd = 2V

The actual lower end of the ICMR for this op amp was 0.7 V, beyond which the NMOS device (M5 in Figure 5.3) in the first gain stage went into the linear region of operation.

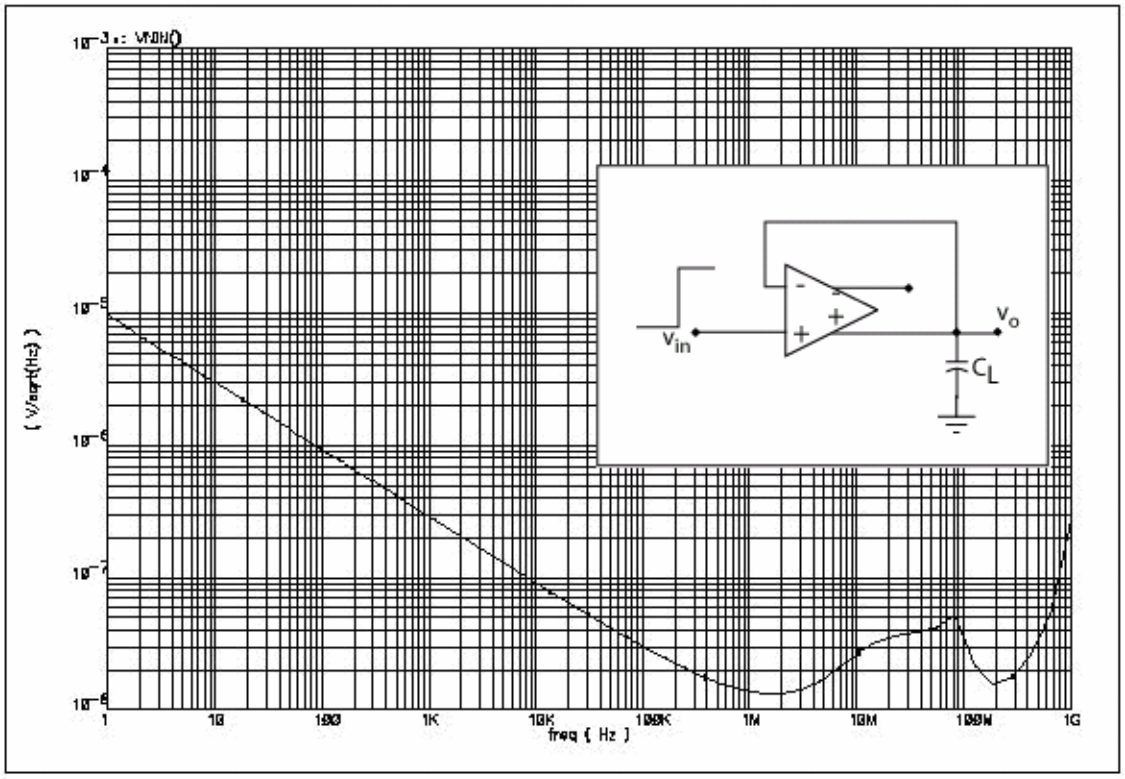


Figure 5.9. Input referred noise of *OP*3 connected as a buffer in the 0.25 μm CMOS process

(Y axis: Input referred noise in $V/\sqrt{Hz}$; X axis: Frequency in Hz)

5.4.2 Simulation Results of *OP*3 in the 0.18 μm CMOS Process

The simulated performance of *OP*3, as a unity-gain buffer, in the 0.18 μm CMOS process (with all 0.35 μm channel length devices) is shown in Table 5.4.

Table 5.4. Simulated performance of *OP*3 in the 0.18 μm CMOS process

Performance specification	**Simulated value**
A_v	96 dB
UGBW (single-ended CL= 1 pF)	80 MHz
Phase margin	84 deg
Slew rate (single-ended CL= 1 pF)	+60,-55 $V / \mu s$
ICMR (Vdd = 1.5 V)	0.45 – 1.1 V
CMRR	93 dB
PSRR	96 dB
Input referred noise	3.8 $\mu V / \sqrt{Hz}$ (1 Hz) 16 $nV / \sqrt{Hz}$ (1 MHz: corner frequency)
Idd	890 μA

The simulation plots for this op amp in the 0.18 μm CMOS process with all 0.35 μm channel length devices are shown next. The op amp was connected in a single-ended, unity-gain configuration.

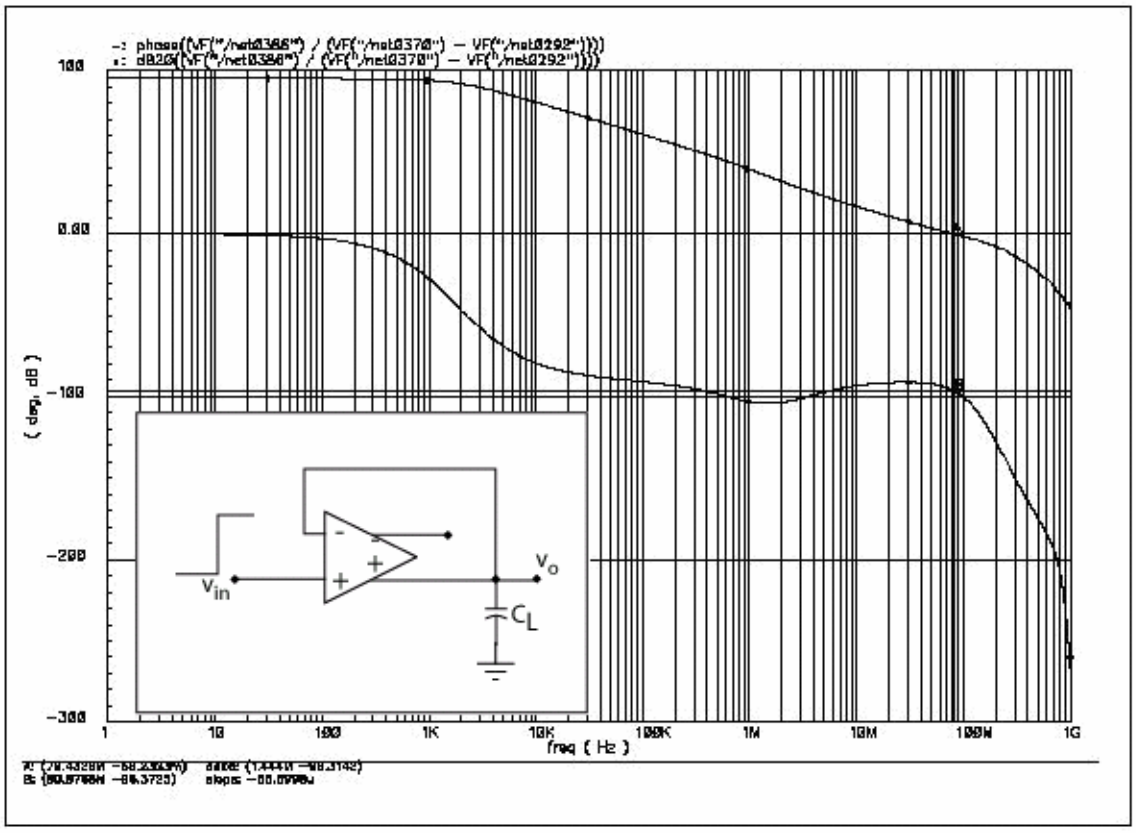


Figure 5.10. Small-signal simulation results of *OP*3 (single ended) in the 0.18 μm CMOS process

(Y axis: Magnitude in dB, Phase in degrees; X axis: Frequency in Hz)

A_v = 96 dB

UGBW (single-ended CL = 1 pF) = 80 MHz

PM = 84 deg

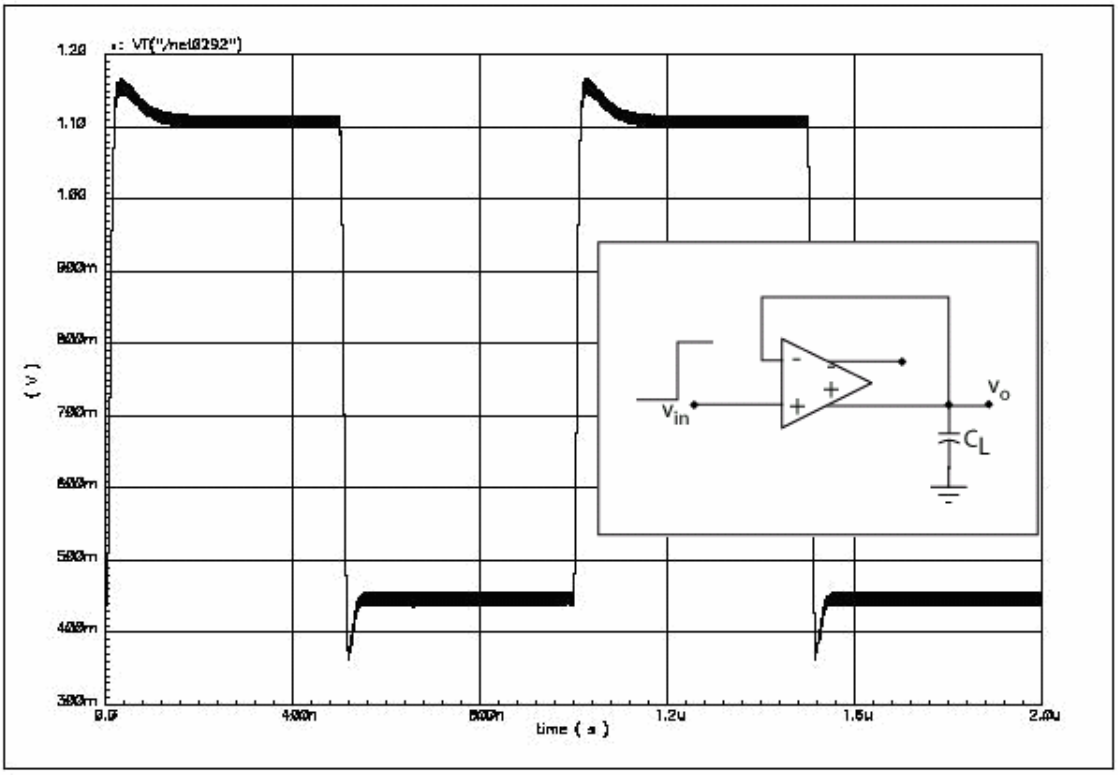


Figure 5.11. Slew rate of *OP*3 connected as a buffer with single-ended load capacitance of 1 pF in the 0.18 μm CMOS process

(Y axes: Output in Volt; X axes: time)

$$SR^{+} = +60 \;\; V / \mu s$$

$$SR^{-} = -55 \;\; V / \mu s$$

In this simulation plot, small oscillations can be seen in the output waveform. These oscillations were caused by an effective negative resistance at the differential outputs of the gain stages for lower input common-mode voltages as explained in Section 4.4.

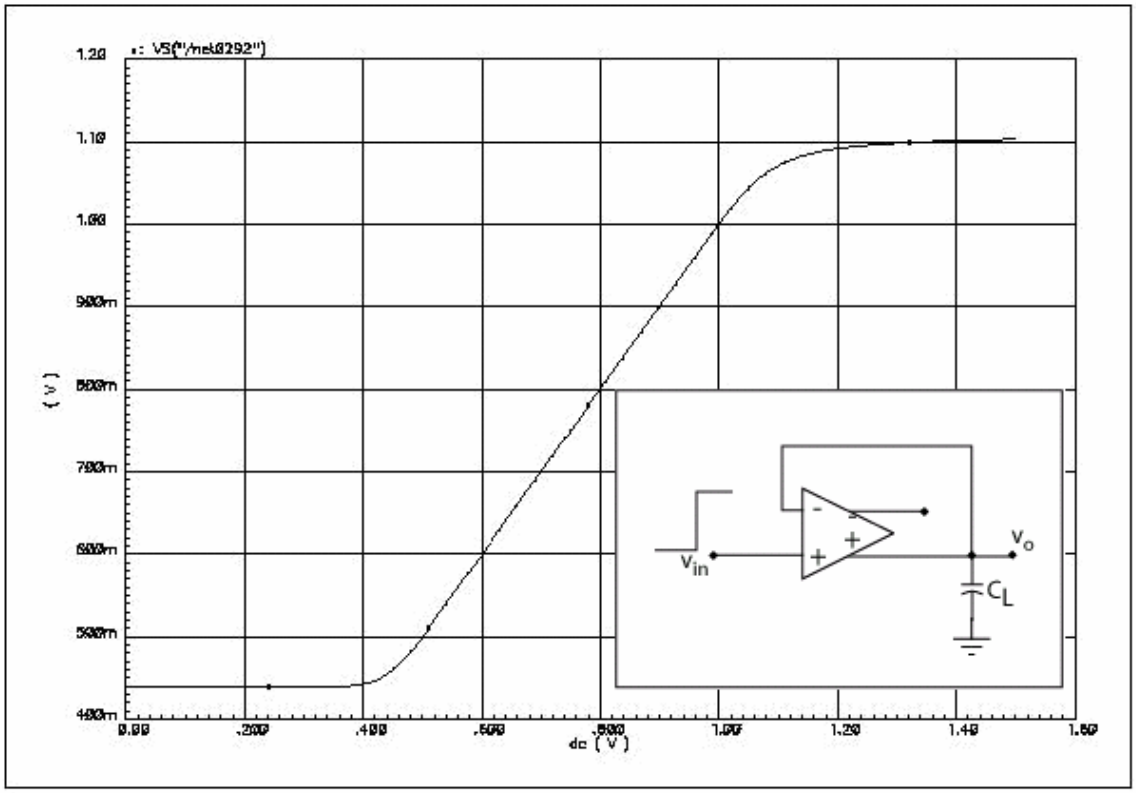


Figure 5.12. Input common-mode range of *OP*3 connected as a buffer in the 0.18 μm CMOS process

(Y axis: Output in Volt; X axis: Input in Volt)

ICMR = 0.45 – 1.1 V

Vdd = 1.5 V

The actual lower end of the ICMR for this op amp was 0.5 V, beyond which the NMOS device (M5 in Figure 5.3) in the first gain stage went into the linear region of operation.

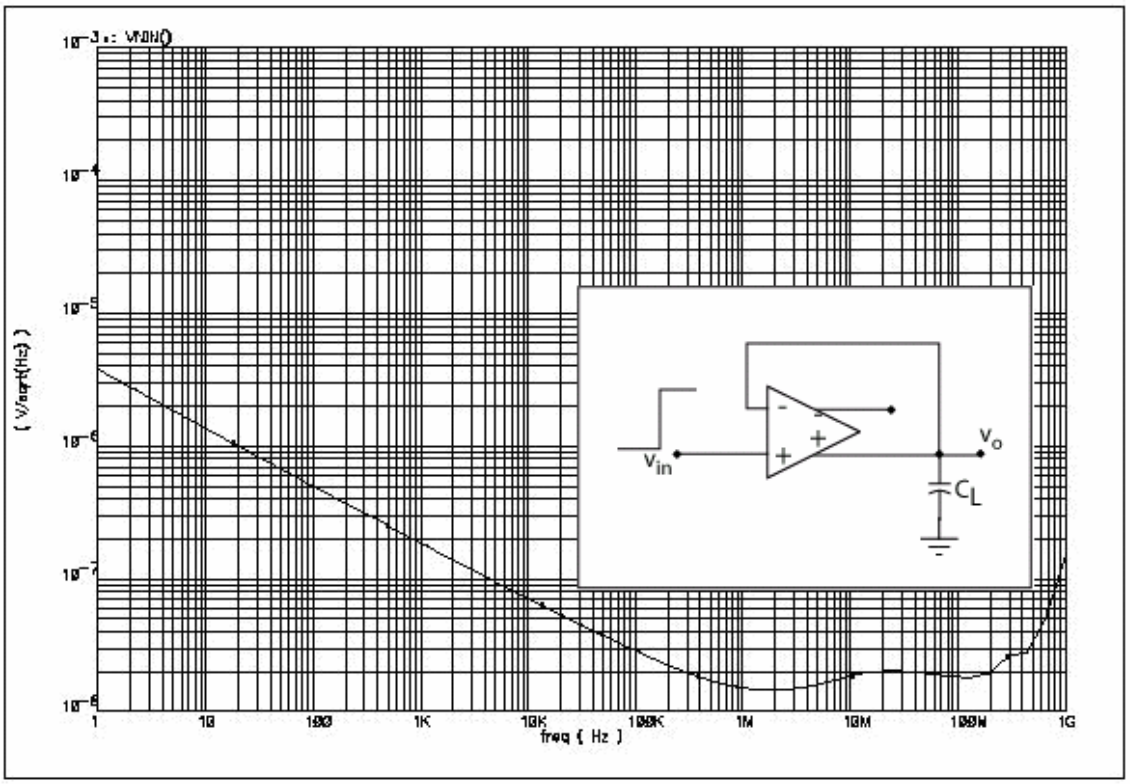


Figure 5.13. Input referred noise of *OP*3 connected as a buffer in the 0.18 μm CMOS process

(Y axis: Input referred noise in $V/\sqrt{Hz}$; X axis: Frequency in Hz)

5.4.3 Comparison of the Simulation Results of *OP*3 in both the CMOS Processes

The simulated performance for *OP*3 in the 0.25 μm CMOS and the 0.18 μm CMOS processes is tabulated next.

Table 5.5. Comparison of the simulated performance of *OP*3 in two different CMOS processes

Performance specification	**Simulated value**	
	0.25 μm CMOS	**0.18 μm CMOS**
Vdd	2 V	1.5 V
A_v	98 dB	96 dB
UGBW (single-ended CL= 1 pF)	60 MHz	80 MHz
Phase margin	92 deg	84 deg
Slew rate (single-ended CL= 1 pF)	+60, -50 $V / \mu s$	+60,-55 $V / \mu s$
ICMR	0.62 – 1.46 V	0.45 – 1.1 V
CMRR	90 dB	93 dB
PSRR	92 dB	96 dB
Input referred noise	9.5 $\mu V / \sqrt{Hz}$ (1 Hz) 14.5 $nV / \sqrt{Hz}$ (2 MHz: corner freq)	3.8 $\mu V / \sqrt{Hz}$ (1 Hz) 16 $nV / \sqrt{Hz}$ (1 MHz: corner freq)
Idd	960 μA	890 μA

In the comparison in Table 5.5, even though different channel lengths were used in both the processes, the aspect ratios of the devices were kept the same resulting in a scalable architecture. The value of A_v in *OP*3 is greatly improved over *OP*2 with the use of twice the channel lengths than the minimum feature sizes. *OP*3 was designed to achieve a constant UGBW and phase margin. For a 1 pF load capacitance, the target value for the UGBW and the phase margin was 66 MHz and 76° respectively. Referring to Table 5.5, though the UGBW and the phase margin are not constant, they are almost equal or better than the target values for which they were designed. They are not constant primarily due to the affect of the pole-zero pair from the buffers in the Miller compensation paths. The UGBW in the 0.25 μm CMOS process was slightly less than the target value because the input transconductance of the op amp is slightly reduced due to bulk effects. The effect of the zero, generated by the unity-gain buffers in Figure 5.4, was negligible in the 0.25 μm CMOS process compared to the 0.18 μm CMOS process. This was because of the buffer transistors, which carried more current and had a larger value of buffer transconductance, $g_{m,buffer}$ in the 0.25 μm CMOS process. The zero from the buffers had more effect in the 0.18 μm CMOS process where the zero caused an increase in the UGBW frequency, which in turn caused a slight decrease in the phase margin. In both cases, the phase margin is better than the target value. The effect of the buffer poles and zeros can be avoided by increasing the bias current through the buffers, which will increase the power consumption.

Comparing the 0.18 μm CMOS process and the 0.25 μm CMOS process, the value of K' used in Equation (5.2) was larger and V_T was smaller in the former process. Thus, in order to generate the same g_m in both the processes, the bias current in the 0.18 μm CMOS process was less than the bias current in the 0.25 μm CMOS process, i.e., the quiescent current carried by all the transistors in the 0.25 μm CMOS process was greater than in the 0.18 μm CMOS process. The positive slew rate was slightly more than the negative slew rate because the PMOS loads had more current sourcing capability than the NMOS current sinking devices in the gain stages.

It can be seen that the flicker noise in the 0.25 μm CMOS process was more than in the 0.18 μm CMOS process. Since the same aspect ratios of the devices were maintained in both the CMOS processes, the area decreased while scaling down from the 0.25 μm CMOS to the 0.18 μm CMOS process. From Equation (2.11), decrease in the area (by a factor of 1.93) should have caused an increase in the flicker noise. But, the gate oxide thickness decreased from 5.5 nm in the 0.25 μm CMOS process to 4.2 nm in the 0.18 μm CMOS process. The flicker noise coefficient "*KF*" also decreased from 0.995 in the 0.25 μm CMOS process to a value of 0.78 in the 0.18 μm CMOS process. The value of K' also increased due to decrease in the gate oxide thickness. Overall, the flicker noise was reduced while moving from the 0.25 μm CMOS process to the 0.18 μm CMOS process. The thermal noise was comparable in both the CMOS processes. In the next sections, the measurement results of *OP3* are presented.

5.5 Measured Results

The measurement results for *OP3* in both the CMOS processes are presented in the following sections. The simulation results confirmed that the op amp was able to achieve large gain and an almost constant UGBW and phase margin across the two CMOS processes. The same results were expected from the measurements, but again, various limitations in fabrication and testing limited the performance of the op amp.

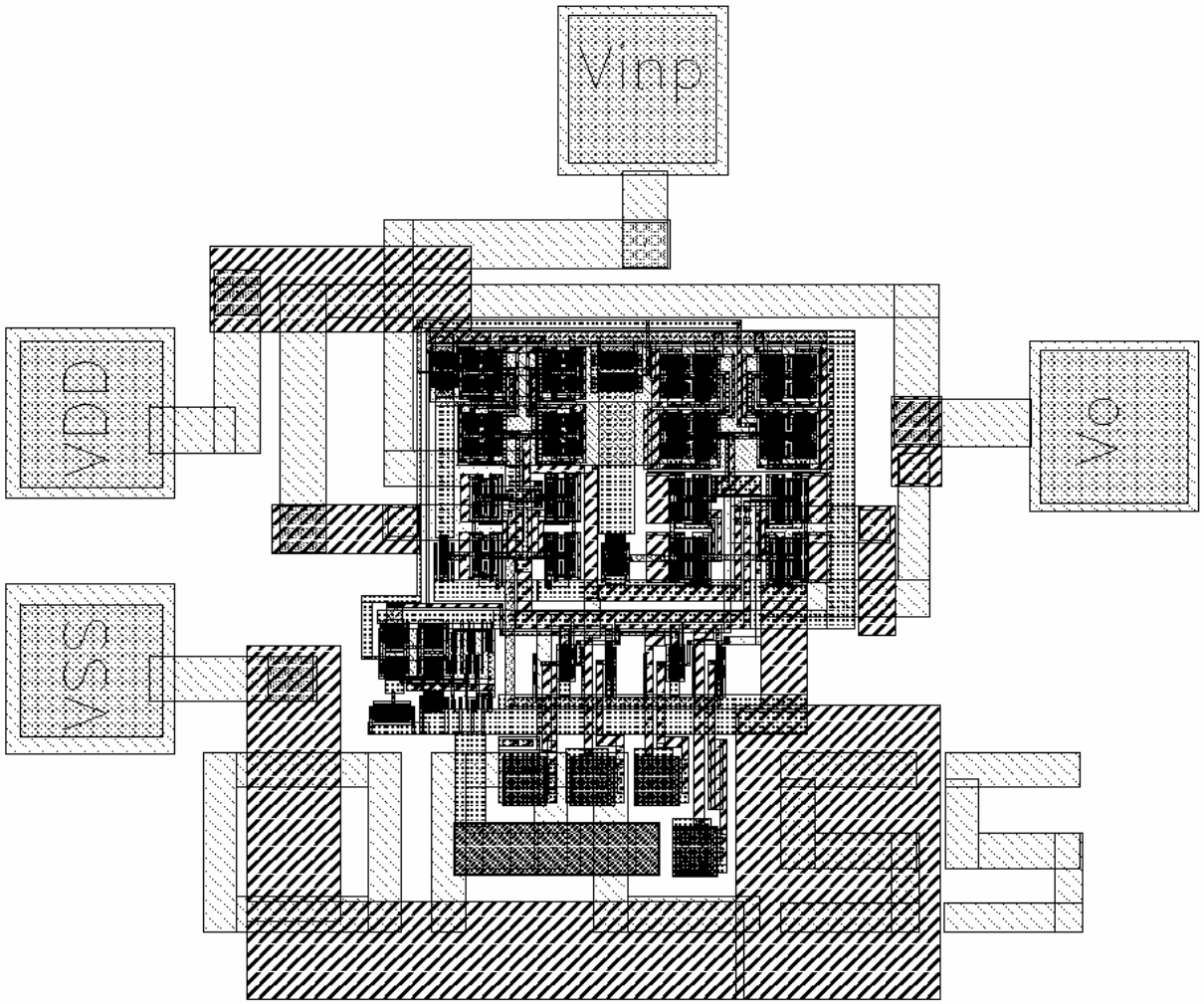


Figure 5.14. Layout of *OP3* in both the CMOS processes

5.5.1 Measured Results of *OP*3 in the 0.25 μm CMOS Process

First, the measured input offset voltage of the op amp with respect to the input common-node voltage is presented in Table 5.6.

Table 5.6. Input offset voltage of *OP3* with input common-mode voltage in the 0.25 μm CMOS process

Vicm (V)	Vos (mV)
0.55	55
0.6	18
0.65	3
0.75	3
0.85	2
0.99	**2**
1.1	4
1.2	5
1.3	5
1.4	11

The nominal input offset voltage was found to be 2 mV. Next, in Table 5.7, a comparison of the simulated and the measured performance of *OP3* in the 0.25 μm CMOS process is presented. Note that during measurements, the output load capacitance was about 20 pF, where as during the design, simulations were performed for a worst-case load of 1 pF. In order to compare the simulated and measured results for the same output load capacitance, the load capacitance in the simulations was increased to 20 pF, and the results are shown in Table 5.7.

Table 5.7. Simulated and measured performance of *OP3* in the 0.25 μm CMOS process

Specifications	Simulated value	Measured value
Channel length (L)	0.55 μm	0.55 μm
VDD (V)	2	2
IDD (mA)	0.95	0.93
Vos (mV)	-	2
Av (dB)	98	-
UGBW (MHz)	20 (CL = 20 pF)	> 10 (CL = 20 pF)
PM (degrees)	60 (CL = 20 pF)	> 70 (CL = 20 pF)
SR ($V / \mu s$)	+4.9, -4.8 (CL = 20 pF)	4 (CL = 20 pF)
ICMR	0.62 – 1.46 V	0.64 – 1.44 V
PSRR (at dc)	92 dB	46 dB for 100 mV change in VDD

This op amp was not packaged, and it was only tested by means of wafer probing, which limited the measurements. The small-signal gain could not be measured as the op amp was fabricated as a unity-gain buffer with its non-inverting output wired to the inverting input internally in the chip. This was done to decrease the capacitive loading at the output. If the op amp was fabricated in the open-loop configuration, then manually short circuiting the output terminal with the inverting input terminal by a co-axial wire would have caused at least 50 pF loading at the output terminal. During measurements using the probe station, the

output load capacitance was about 20 pF, which affected the ac and transient performance. The UGBW could not be measured fully using a network analyzer due to limitations imposed by losses in the coaxial cables during wafer probing. An attempt was made to measure the UGBW frequency by observing the time domain output response for sinusoidal input with different frequencies, but this technique did not work beyond 10 MHz due to excessive noise in the probe setup. The PSRR measurement was done at dc for a 100 mV change in VDD, which was not a small-signal change. Thus, its measured value was much smaller than the simulated value, which was true for a small-signal "ac" change in the VDD. The measurement plots are shown next.

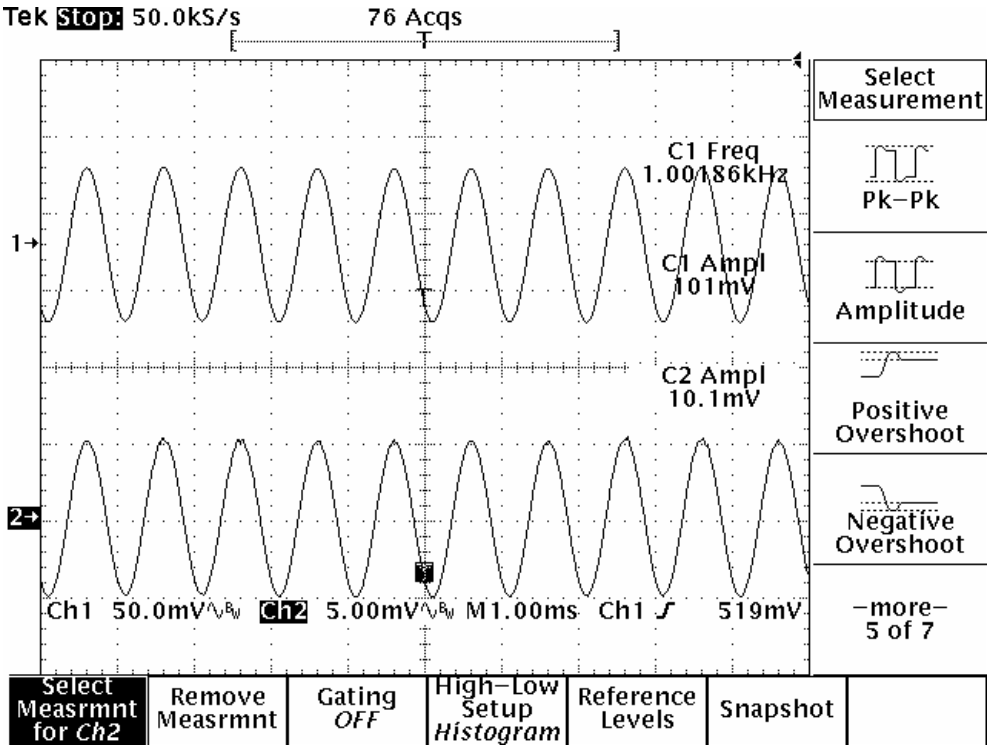


Figure 5.15. Time domain input (Ch1) and output (Ch2) waveforms of *OP3* connected as a unity gain buffer in the 0.25 μm CMOS process

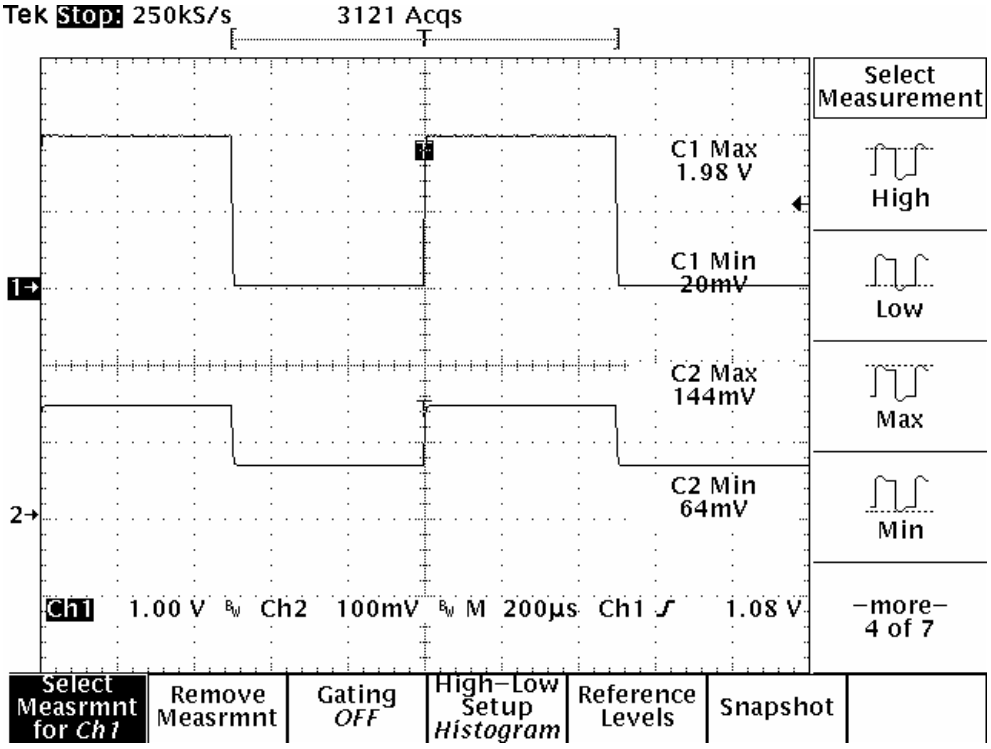


Figure 5.16. ICMR of the *OP3* in the 0.25 μm CMOS process

The input (Ch1) is a 0 – 2 V pulse, and the output (Ch2) swings between 0.64 – 1.44 V, which is a measure of the ICMR of the op amp. The output (Ch2) has a 10X attenuation.

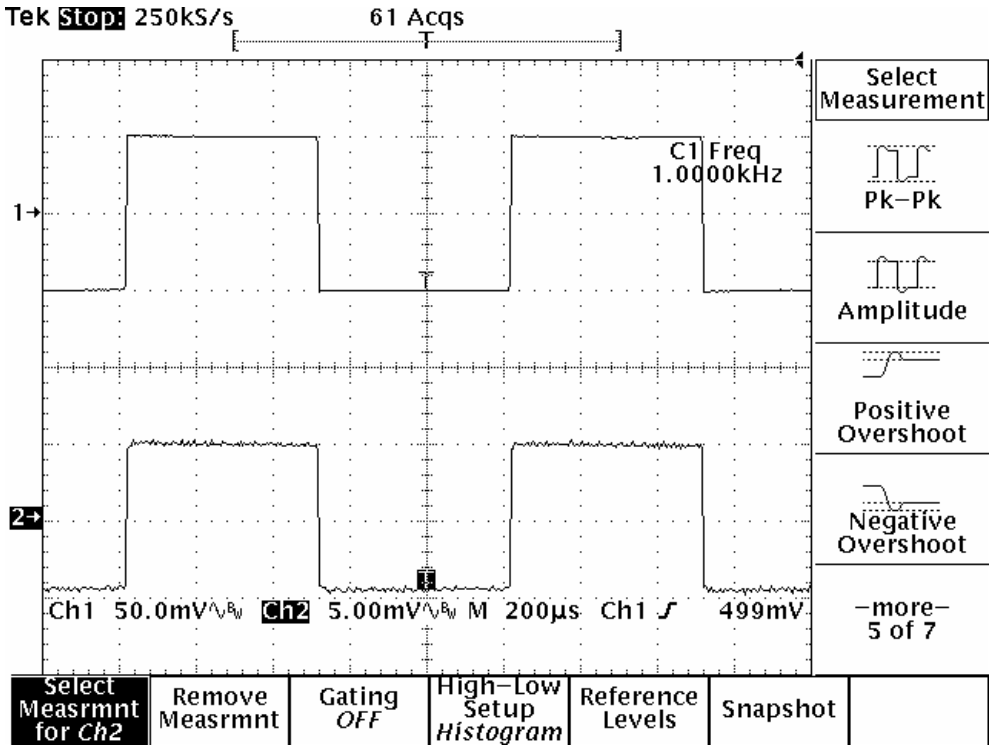


Figure 5.17. Phase margin of *OP3* in the 0.25 μm CMOS process

The phase margin of this op amp was greater than 70 degrees because the overshoot is practically negligible (less than 10%). The output load capacitance was 20 pF.

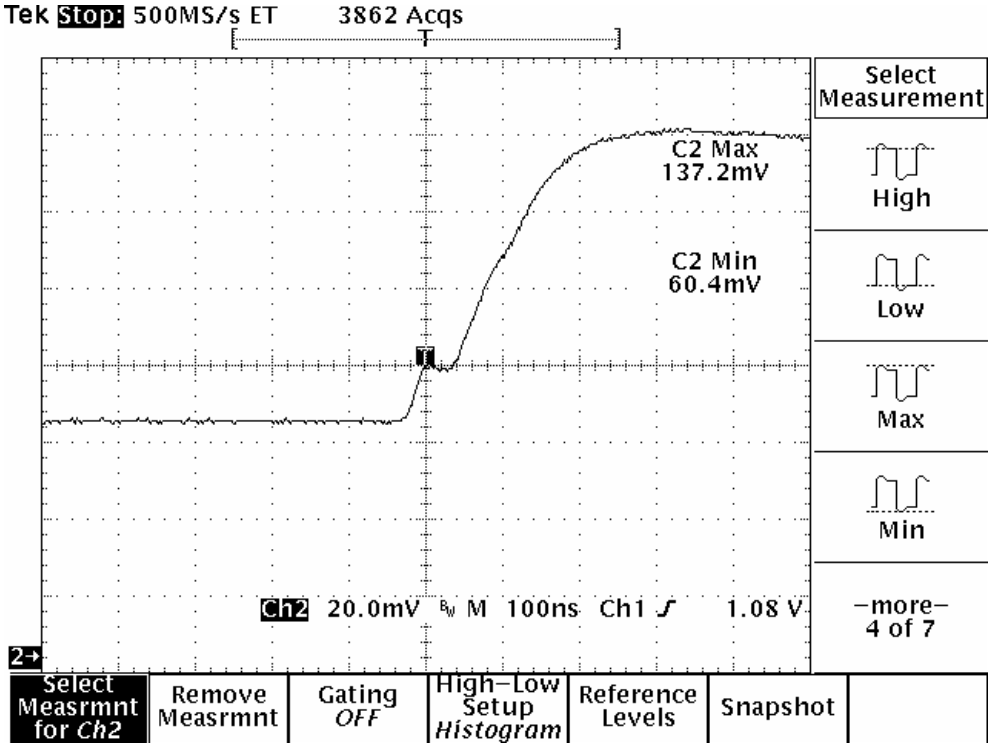


Figure 5.18. SR of the *OP3* in the 0.25 μm CMOS process

The SR of the op amp was about 4 V/us for a CL of 20 pF. The large-signal slewing of the op amp was primarily limited by the output load capacitance. When the op amp starts to slew positive, a small initial jump in the output can be seen in this plot. It was most probably caused by the finite coupling capacitance between the input and the output lines (both in the layout and in the test setup), which formed a capacitive divider with the output load capacitance.

5.5.2 Measured Results of *OP*3 in the 0.18 μm CMOS Process

First, the measured input offset voltage of the op amp with respect to the input common-node voltage is presented in Table 5.8. Its nominal value was 1 mV.

Table 5.8. Input offset voltage of *OP3* with input common-mode voltage in the 0.18 μm CMOS process

Vicm (V)	**Vos (mV)**
0.5	29
0.55	17
0.6	5
0.7	**3**
0.8	**1**
0.9	1
1.0	-1
1.1	-5
1.15	-22
1.2	-67

Next, in Table 5.9, a comparison of the simulated and the measured performance of *OP3* in the 0.18 μm CMOS process is presented. Note that during measurements, the output load capacitance of the measurement setup was about 20 pF. Thus, in the simulation results, the output load capacitance was also set at 20 pF in order to compare with the measurement results.

Table 5.9. Simulated and measured performance of *OP3* in the 0.18 μm CMOS process

Specifications	Simulated value	Measured value
Channel length (L)	0.35 μm	0.35 μm
VDD (V)	1.5	1.5
IDD (mA)	0.89	0.9
Vos (mV)	-	1
Av (dB)	96	-
UGBW (MHz)	22 (CL = 20 pF)	> 10 (CL = 20 pF)
PM (degrees)	65 (CL = 20 pF)	> 70 (CL = 20 pF)
SR ($V / \mu s$)	5 (CL = 1 pF)	5 (CL = 20 pF)
ICMR	0.45 – 1.1 V	0.46 – 1.14 V
PSRR (at dc)	96 dB	46 dB for 100 mV change in VDD

Just like in the 0.25 μm CMOS process, this op amp was not packaged, and it was only tested by means of wafer probing, which limited the measurements. The small-signal gain could not be measured as the op amp was fabricated as a unity-gain buffer with its non-inverting output wired to the inverting input. During measurements using the probe station, the output load capacitance was about 20 pF, which affected the ac and transient performance. The UGBW could not be measured fully due to limitations imposed by losses in the coaxial cables during wafer probing. The PSRR measurement was done at dc for a 100 mV change in

VDD, which was not a small-signal change. Thus, its measured value was much smaller than the simulated value, which was true for a small-signal "AC" change in the VDD. The measurement plots are shown next.

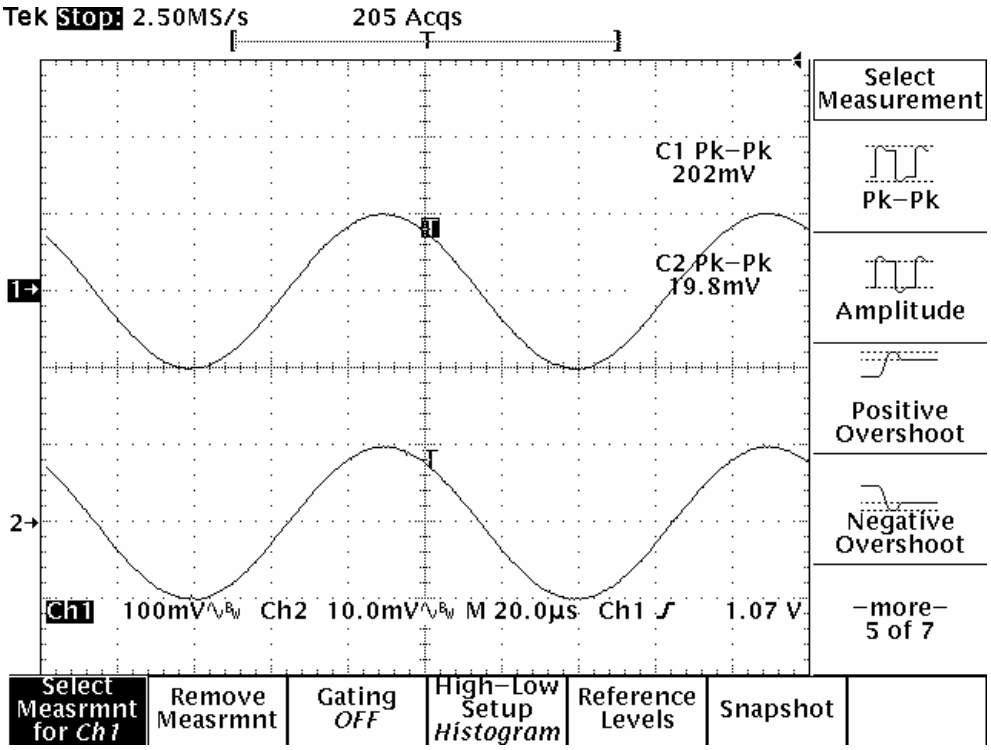


Figure 5.19. Time domain input (Ch1) and output (Ch2) waveforms of *OP3* connected as a unity gain buffer in the 0.18 μm CMOS process

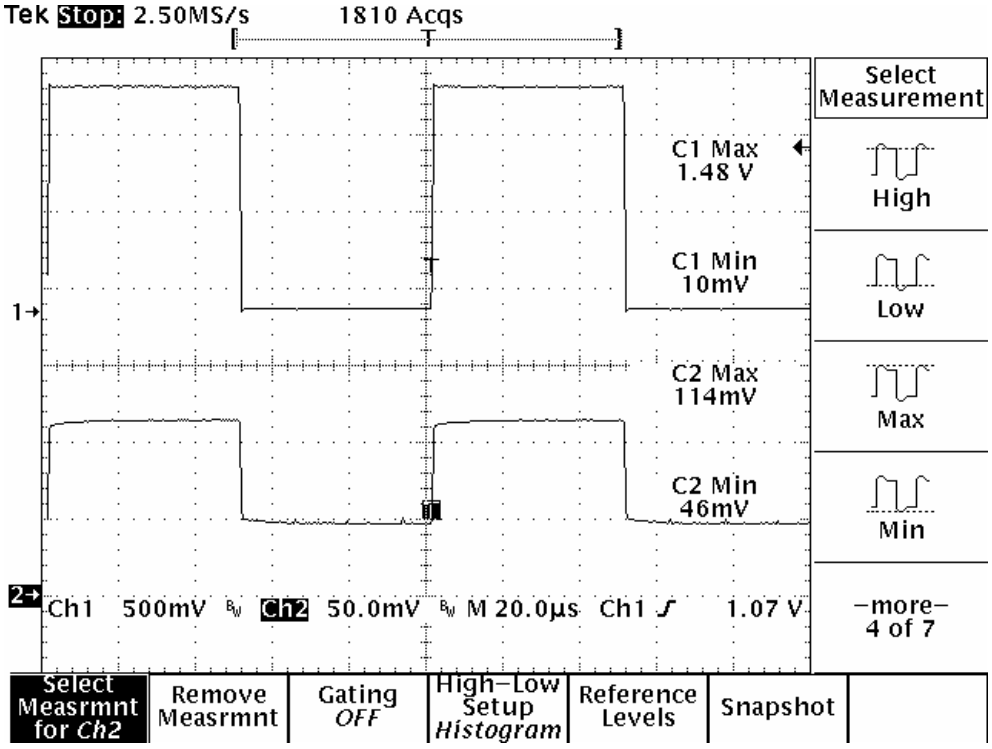


Figure 5.20. ICMR of *OP3* in the 0.18 μm CMOS process

The input (Ch1) is a 0 – 1.5 V pulse, and the output (Ch2) swings between 0.46 – 1.14 V, which is a measure of the ICMR of the op amp.

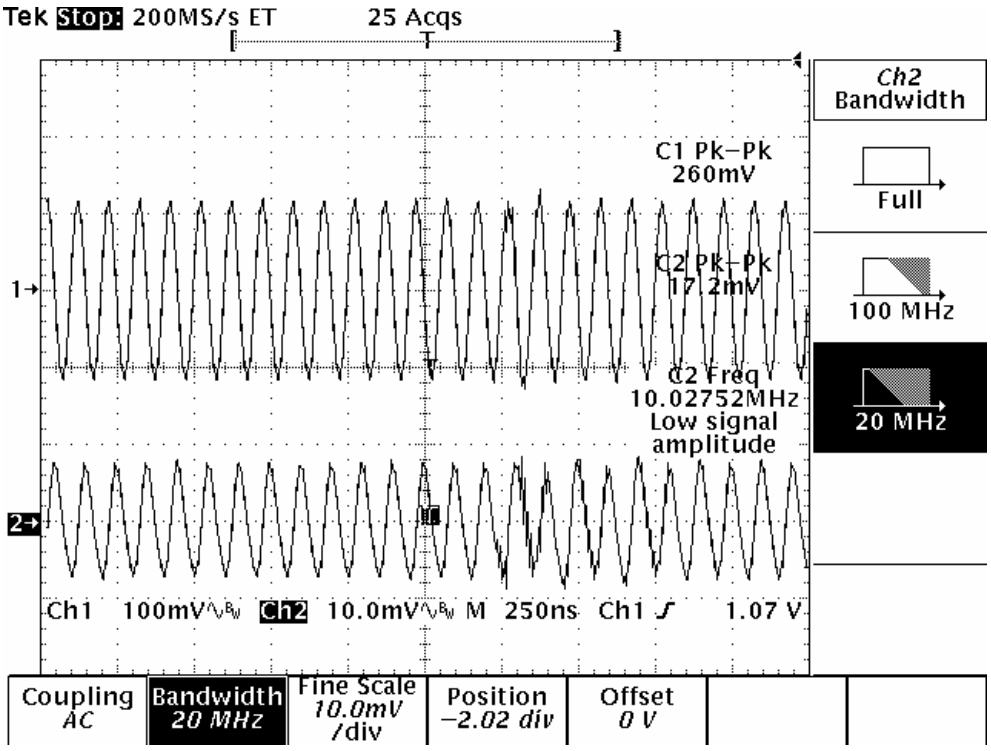


Figure 5.21. Input (Ch2) and output (Ch1) waveforms of *OP3* for a 10 MHz sinusoidal input in the 0.18 μm CMOS process

This part was not packaged, and it was only tested by means of wafer probing. The UGBW frequency is greater than 10 MHz. The function generator was limited up to 10 MHz, beyond which its output became too noisy, and the noise of the probe setup became significant compared to the small-signal input.. In this measurement, the output CL was about 20 pF. Attempt was also made to measure the UGBW frequency using a network analyzer and a spectrum analyzer, but the losses associated with the coaxial cables, used in the probing of the die, was too large to measure the UGBW frequency.

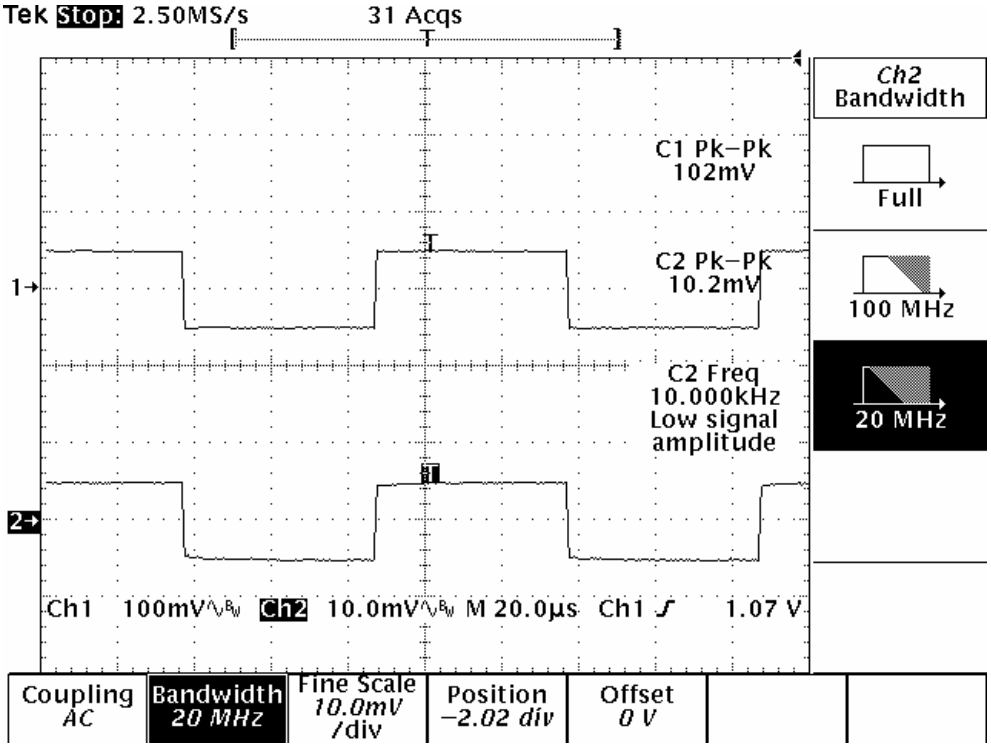


Figure 5.22. Phase margin of *OP3* in the 0.18 μm CMOS process

The phase margin of this op amp was greater than 70 degrees because the overshoot is practically negligible (less than 10%). The output load capacitance was 20 pF.

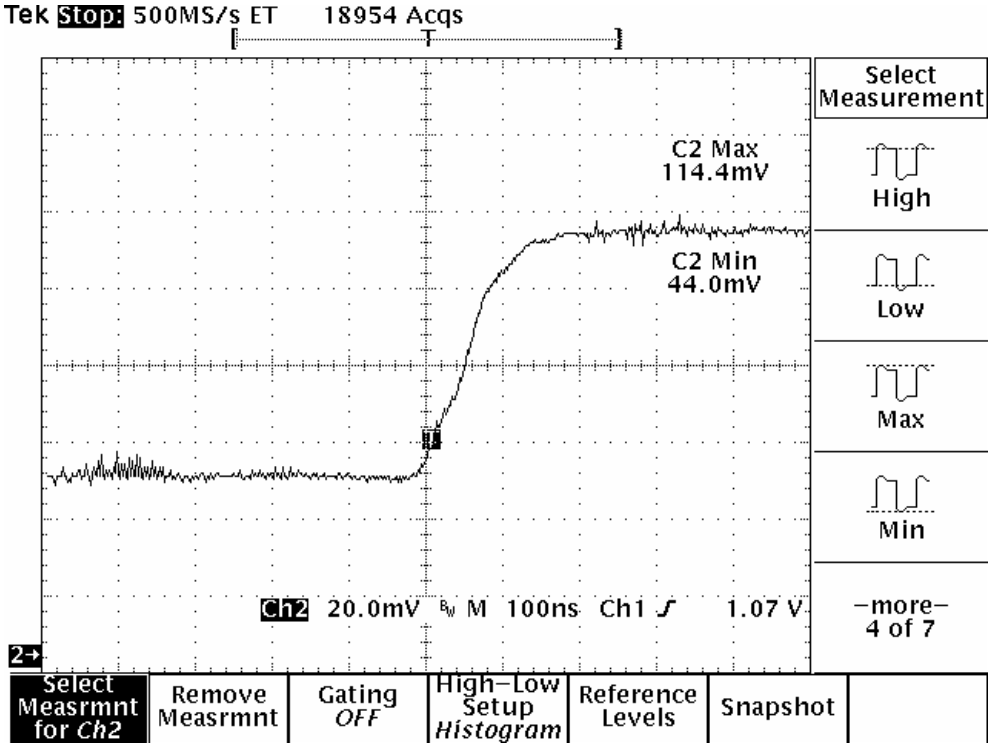


Figure 5.23. SR of *OP3* in the 0.18 μm CMOS process

The SR of the op amp was about 5 V/us for a CL of 20 pF. The large-signal slewing of the op amp was primarily limited by the output load capacitance.

5.6 Summary

The design of an op amp, *OP3*, with constant UGBW frequency and phase margin was presented in this chapter. The UGBW frequency of the op amp depends on the input transconductance of the differential input pair. Using a Bootstrap biasing scheme, constant transconductance was generated, which was intended for the design of constant UGBW frequency of the op amp. This op amp was designed using devices with twice the minimum feature-size channel lengths. A simple biasing scheme was used to generate and mirror the bias currents into the devices, and all the NMOS and PMOS bulks were kept reversed biased. The simulated and measured results of *OP3* were presented. This op amp was designed to achieve:

1. Large small-signal gain
2. Constant UGBW frequency
3. Constant phase margin.

The simulation results show that the above three objectives were met with the same circuit scaled from the 0.25 μm CMOS and the 0.18 μm CMOS processes. During measurements, this op amp could not be packaged, and it was measured using wafer probes, which limited the scope of the measurements. The small-signal gain could not be measured during wafer probing because the op amp was connected as a unity-gain buffer internally inside the chip. The output load capacitance was larger than the maximum designed load capacitance. Still, the op amp showed comparable phase margins, which were greater than 70 degrees in both the CMOS processes. The UGBW frequency could not be measured due to

limitations of the measurement setup. Overall, the affect of scaling on the performance of the op amp architecture from one technology to the other was partially verified within the limitations of measurements.

Even though the gain, UGBW, and phase margin of the op amp needed to be compared to prove scalability across technologies, only the phase margin could be verified through a comparison of their small-signal response, which is shown in Figure 5.24. The gain and the UGBW could not be compared in both the CMOS processes.

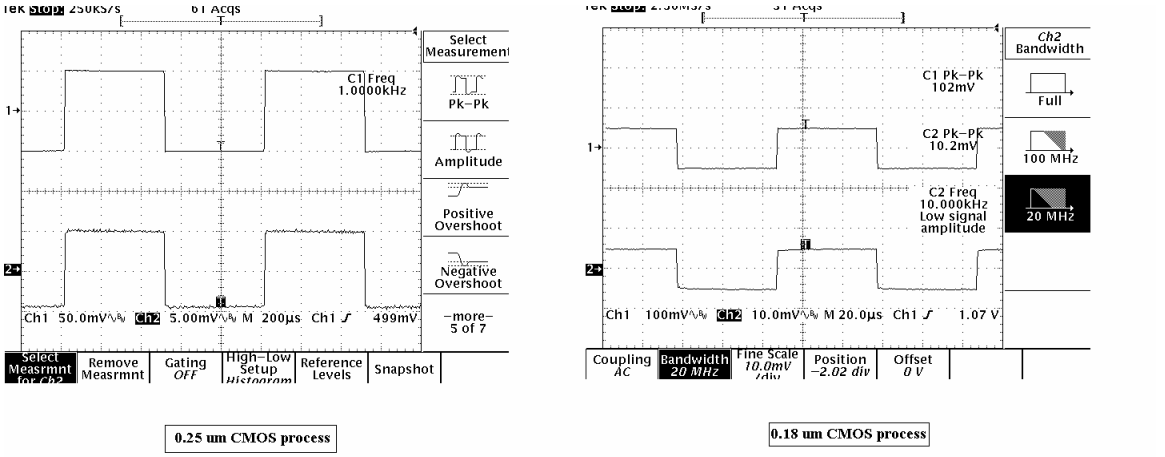


Figure 5.24. Comparison of the overshoot and phase margins in the small-signal response of *OP2* in both the CMOS processes

In the next chapter, buffered versions of these op amps are developed such that their outputs can be buffered by source followers to drive large output capacitive loads. The output buffer will be designed as a g_m boosted source follower using current feedback capable of driving capacitively coupled 50 Ω output loads with large output capacitances.

Chapter 6

Buffered Op Amps

In the previous chapters, scalable op amps were developed to achieve large gain, and constant UGBW frequency and phase margin independent of the technology and the channel length. These op amps consisted of two cascaded gain stages, which can be viewed as "un-buffered" op amps as their output impedance was large. They were designed for small output load capacitance (up to 2 pF), but during measurements, the output load capacitance was 20-50 times larger than the designed value. Thus, it is important to develop "buffered" versions of these op amps, such that they will be able to drive large output load capacitances. Moreover, during measurements, some of the instruments had 50 Ω input resistance, which made the buffering of the outputs of these op amps a necessity.

In designing "buffered" op amps, compensation becomes important. Mostly, a source follower follows the two gain stages, which acts as the final stage of the "buffered" op amp. Addition of the source follower adds its own pole-zero pair; the pole being more dominant over the zero for large load capacitance. This converts the small-signal transfer function of the op amp from a 2 pole to a 3 pole system, which affects the phase margin and the closed loop settling response of the op amp. It is desired that the extra pole (or poles) caused by the addition of the output buffer stage in the op amp should be much larger so as not to influence the gain or the phase responses up to the UGBW frequency. In the case of the output buffer stage being implemented using source followers,

their poles can be kept large by burning more power in the source followers, which will not give a low power solution. Another possible option can be to use feedback to boost the effective transconductance of the source follower with smaller bias currents. Such a technique is discussed next, where the effective transconductance of the source follower is boosted using current feedback. The proposed scheme is similar to the one used in [47], where the effective transconductance was boosted by controlled positive voltage feedback.

6.1 Current Feedback g_m Boosted PMOS Source Follower with NMOS Current Mirror Sink

In order to buffer the outputs of *OP2* and *OP3* by source followers, there are two primary requirements:

1. The output source followers should be able to drive capacitively coupled 50 Ω output resistance with appreciable source follower gain, such that the overall gain of the op amp is not degraded.
2. The pole(s) introduced by the source followers should be much larger (about 5 – 10 times) than the largest pole that effect the UGBW frequency and the phase margin.

These two requirements can be met by developing a source follower whose effective transconductance is boosted by current feedback, and such an architecture is shown in Figure 6.1. In this figure, a single-transistor PMOS source follower is modified into a three-transistor source follower by the addition of the NMOS current mirror. The output load resistance and capacitance are de-

coupled using a blocking capacitor Cb. It will be assumed that the bulk (n-well) and the source terminals of the PMOS devices are tied together.

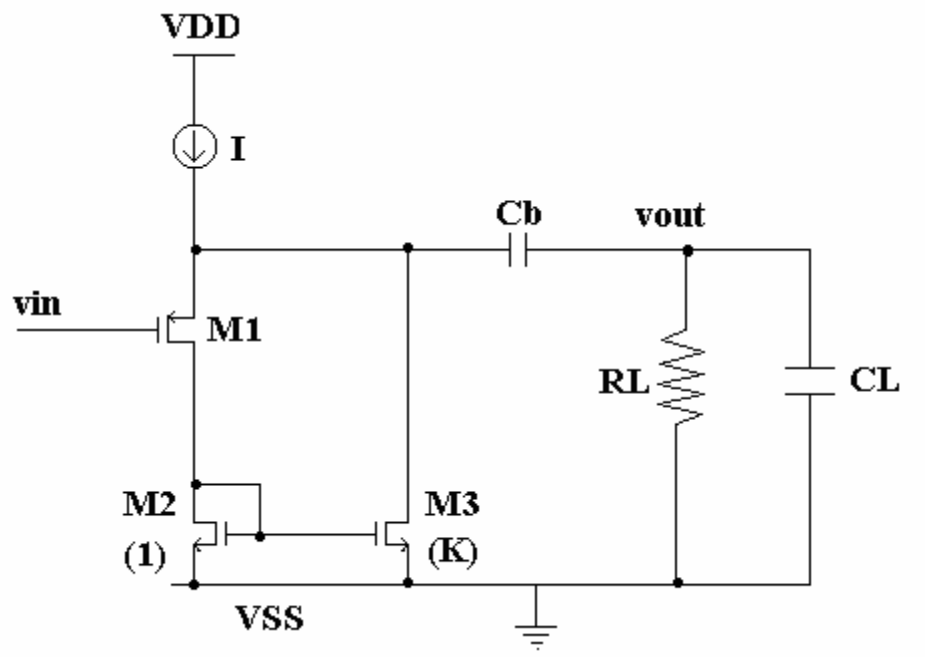


Figure 6.1. Current feedback g_m boosted "modified" PMOS source follower with NMOS current mirror sink

A quick look at Figure 6.1 shows that M1-M2-M3 form a negative current feedback loop, whose loop-gain is (-K). The total bias current "I" is distributed into two branches: one through M1 and the other through M3 as

$$I_1 = \frac{I}{(K+1)} \tag{6.1}$$

$$I_3 = \frac{I(K)}{(K+1)} \tag{6.2}$$

If we compare the PMOS source follower transistor (M1) in Figure 6.1 with a simple, single transistor PMOS source follower, one can see that the current

through M1 is reduced by a factor of (K+1) in the former case. Assuming a square law device, this will correspond to a decrease in g_{m1} by a factor of $\sqrt{K+1}$. But, due to the 1:K NMOS current mirror, the total small-signal current at the output is (K+1) times the small-signal current carried by M1. Thus, the effective small-signal output current and the transconductance of the source follower is boosted by a factor of $\sqrt{K+1}$ compared to a simple source follower.

Let us develop various expressions for the source follower shown in Figure 6.1.

a) Small-signal output current and effective transconductance

The small-signal output current can be given by

$$i_{out} = (K+1)i_1 = \{(K+1)g_{m1}\}(v_{in} - v_{out}) \tag{6.3}$$

Equation (6.3) will give the effective transconductance as

$$g_{m,eff} = (K+1)g_{m1} = \sqrt{2K'\left(\frac{W}{L}\right)_1 (K+1)I} \tag{6.4}$$

From Equation (6.4), an interesting point to note is that the effective transconductance of the modified source follower will be equal to the transconductance of a single-transistor source follower, which either has its bias current or its aspect ratio scaled by a factor of (K+1). This shows that the modified source follower can achieve lower area as well as power.

b) Small-signal gain

The mid band, small-signal gain of the modified source follower in Figure 6.1 can be expressed as

$$A_V = \frac{g_{m,eff}}{\left[g_{m,eff} + \frac{1}{R_L} + g_{ds1}\left(1 + \frac{1}{g_{m2} R_L} \right) \right]} \tag{6.5}$$

It can be seen that the small-signal gain is slightly degraded due to the low-impedance node caused by the diode-connected M2. But, the overall small-signal gain is improved compared to a simple source follower due to boost in the effective transconductance.

c) Small-signal output resistance

The small-signal output resistance is improved due to current feedback, and it can be given by

$$R_{out} = \frac{1}{\left[g_{m,eff} + \frac{1}{R_L} + g_{ds1}\left(1 + \frac{1}{g_{m2} R_L} \right) \right]} \tag{6.6}$$

d) Frequency response

The single-transistor source follower has a single pole-zero pair, both of which are dependent on the transconductance of the source follower. In Figure 6.1, a boost in the transconductance will surely push out the pole, but other poles and zeros will also appear in the overall transfer function. The small-signal transfer function of the circuit in Figure 6.1 can be derived, and simplification of the transfer function will lead to two major poles as

$$p_1 = -\frac{\left[g_{m,eff} + \frac{1}{R_L} + g_{ds1}\left(1 + \frac{1}{g_{m2} R_L} \right) \right]}{C_L} \tag{6.7}$$

$$p_2 \cong -\frac{g_{m2}}{(K+1)C_{gs2}} \tag{6.8}$$

A single-transistor source follower has only one pole at the output, but the modified source follower of Figure 6.1 has two major poles. The first pole, given by Equation (6.7) is pushed out due to boost in the effective transconductance, which improves the bandwidth of the source follower. The second pole, given by Equation (6.8) needs to be larger than the first pole. In a CMOS process, the parameter f_T is defined as

$$f_T = \frac{g_m}{C_{gs}} \tag{6.9}$$

A careful look at Equation (6.8) shows that the second pole is approximately (K+1) times smaller than f_T, which is in the order of few GHz in the present day CMOS processes. Thus, in most cases, the second pole will be larger than the first pole.

In this design, there is a trade off between the location of the second pole and the boost in the effective transconductance. The loop gain of the current feedback loop is

$$|LG| = \frac{g_{m3}}{g_{m2}} \tag{6.10}$$

Equation (6.8) gives the expression for the second pole, which can be written as

$$p_2 = -\frac{g_{m2}}{C_{gs3} + C_{gs2}} \tag{6.11}$$

The product of the loop gain and the second pole is

$$\left|(LG)p_2\right| \cong \frac{g_{m3}}{C_{gs3}} \cong f_T \tag{6.12}$$

Equation (6.12) shows that there exists a trade off between the loop gain and the second pole, and the effective transconductance is dependent on the loop gain. Thus, it might not be possible to boost the effective transconductance largely if the location of the second pole becomes important in the design.

e) Input capacitance

The input capacitance of the source follower is of important concern if it has to be cascaded with the gain stages of the op amp because the input capacitance of the source follower acts as the load capacitance for the second gain stage. If this capacitance is large, it will affect the phase margin of the overall op amp. As stated earlier, one of the advantages of the modified source follower of Figure 6.1 is that one can achieve the same value of effective transconductance as a single-transistor source follower with almost (K+1) times smaller input device size. This helps in reducing the input capacitance, which can be expressed as

$$C_{in} = (1 - A_V)C_{gs1} + \left(1 + \frac{(1 - A_V)g_{m1}}{g_{m2}}\right)C_{gd1} \tag{6.13}$$

The input capacitance of the modified source follower is comparable to the input capacitance of a single transistor source follower.

f) Distortion

In general, the distortion of the buffered op amps are limited by the distortion performance of the output buffers. It can be reduced using cascode

output structures as proposed in [48, 49], but still, the overall distortion of the un-buffered op amps are much smaller than the buffered op amps. Some of the design techniques to reduce distortion were shown in [50]-[52].

In Figure 6.1, it can be seen that the voltage drop across diode-connected M2 tends to decrease V_{ds1}, which will push M1 out of saturation into linear region of operation. This is a direct indication that the modified source follower will have poor input signal handling capacity and large distortion effects. In general, the higher order harmonics will tend to become stronger with

i. Decrease in r_{ds1}, which will decrease the small-signal gain

ii. Decrease in the load resistance

iii. Decrease in the bias current, I, for large positive output swing.

This source follower is good only for small-signal inputs. This technique of boosting the transconductance using current feedback can be extended to a push-pull source follower, which will be able to handle large-signal inputs. Such a source follower will be discussed in Section 6.3.

The performance of the modified source follower is improved due to boost in the effective transconductance. Its merits will become more prominent if it is compared with a single-transistor source follower with only one PMOS device. If we assume that the total bias current, I, and the aspect ratio of the input PMOS device is kept the same in both the single transistor and modified source followers, then Table 6.1 shows a comparison of their performances.

Table 6.1. Comparison of the performance of the simple, single transistor source follower and the modified, three transistor source follower for the same input device size and total current

Specification	**Single Transistor Source Follower**	**Modified Source Follower**
g_m	g_{m1}	$\left(\sqrt{1+K}\right)g_{m1}$
A_v (mid band)	$\dfrac{g_{m1}}{g_{m1}+\dfrac{1}{R_L}}$	$\dfrac{g_{m1}\left(\sqrt{1+K}\right)}{g_{m1}\sqrt{(1+K)}+\dfrac{1}{R_L}+g_{ds1}\left(1+\dfrac{1}{g_{m2}R_L}\right)}$
BW	$\dfrac{\left(g_{m1}+\dfrac{1}{R_L}\right)}{C_L}$	$\dfrac{g_{m1}\sqrt{(1+K)}+\dfrac{1}{R_L}+g_{ds1}\left(1+\dfrac{1}{g_{m2}R_L}\right)}{C_L}$
R_{out}	$\dfrac{1}{g_{m1}+\dfrac{1}{R_L}}$	$\dfrac{1}{g_{m1}\sqrt{(1+K)}+\dfrac{1}{R_L}+g_{ds1}\left(1+\dfrac{1}{g_{m2}R_L}\right)}$
C_{in}	$(1-A_v)C_{gs1}+C_{gd1}$	$(1-A_V)C_{gs1}+\left(1+\dfrac{(1-A_V)g_{m1}}{g_{m2}}\right)C_{gd1}$

The modified source follower, shown in Figure 6.1, was designed in the 0.18 μm CMOS process. It was specifically designed to drive 50 Ω output load resistance, and a 10 pF load capacitance. A 50 Ω resistance corresponds to a conductance of 20 mS. In order to achieve a minimum small-signal gain of 0.5, the effective conductance of the source follower should be at least 20 mS, which for a MOS device requires large current as well as aspect ratio. Simulation results for the single transistor and modified source followers are shown next in Table 6.2. In this simulation, the total bias current and the input device size was kept the same. For the modified source follower in Figure 6.1, the value of the NMOS current mirror ratio "K" was chosen as 4. This indicates that the effective transconductance will be improved by a factor of approximately $\sqrt{5}$. In Table 6.2, it can be seen that it did improve approximately by a factor of 2. The improvements in the simulated small-signal gain and bandwidth of the modified source follower were 1.3X and 1.5X respectively over the single transistor source follower. As expected, the THD (total harmonic distortion) of the modified source follower was worser than the single transistor source follower. The simulated frequency responses are shown in Figure 6.2

Table 6.2. Comparison of the simulation results of the single transistor and modified source followers

Specification	**Single Transistor Source Follower**	**Modified Source Follower**
Total bias current	4 mA	4 mA
Effective g_m	20.6 mS	41 mS
A_V (mid-band)	-6.2 dB	-4 dB
BW	630 MHz	938 MHz
R_{out}	48.5 Ω (without RL) 24.6 Ω (with RL)	24.4 Ω (without RL) 16.4 Ω (with RL)
C_{in}	150 fF	145 fF
THD (Vin=100 mVp-p)	1.3%	2.5%

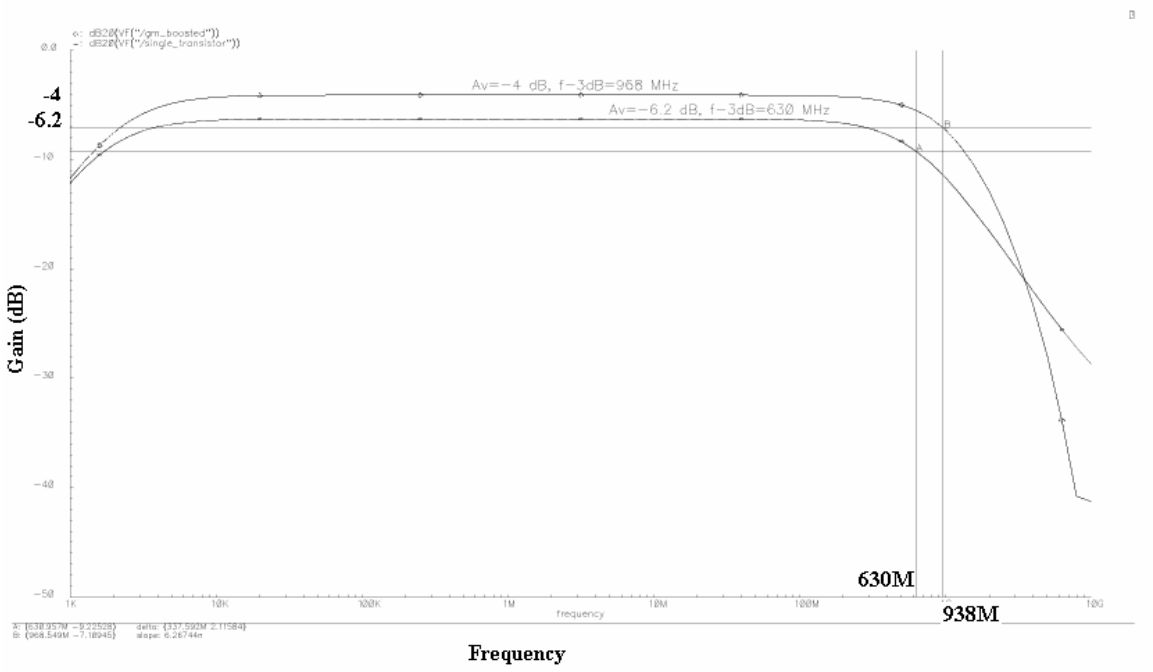


Figure 6.2. Simulated frequency response of the single transistor and modified source followers

The modified source follower had larger small-signal gain as well as bandwidth compared to the single-transistor source follower. Notice that the single-transistor source follower has a single-pole frequency roll-off, where as the modified source follower has a two-pole frequency roll-off. The low-frequency roll-off is caused by the DC blocking capacitor at the output.

6.2 Current Feedback g_m Boosted PMOS Source Follower with Resistor-NMOS Sink

In Figure 6.1, a g_m boosted PMOS source follower was described. The same circuit can be modified by replacing the NMOS device M2 by a resistor, and it is shown in Figure 6.3.

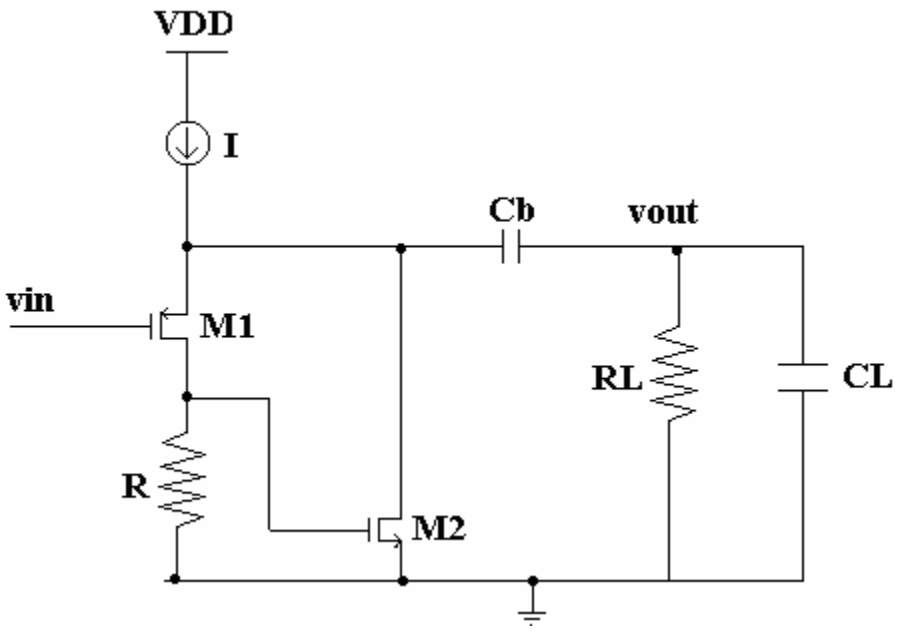


Figure 6.3. Current feedback g_m boosted "modified" PMOS source follower using resistor-NMOS sink

The advantage of going from the circuit in Figure 6.1 to the circuit shown above in Figure 6.3 is that the voltage drop across the resistor can be made less as compared to the V_{gs} drop of the diode connected NMOS device M2 in Figure 6.1, which will improve the THD performance.

For the circuit in Figure 6.3, the biasing currents through M2 can be found as

$$I_2 = K'\left(\frac{W}{L}\right)_2 \frac{(V_{gs2} - V_{T2})^2}{2} \tag{6.14}$$

or, $$I_2 = K'\left(\frac{W}{L}\right)_2 \frac{((I - I_2)R - V_{T2})^2}{2} \tag{6.15}$$

Solving the quadratic equation in Equation (6.15) will give I_1 and I_2 as

$$I_2 = I - \left[\frac{V_{T2}}{R} + \frac{1}{K'\left(\frac{W}{L}\right)_2 R^2}\left\{\sqrt{2K'\left(\frac{W}{L}\right)_2 R(IR - V_{T2}) + 1} - 1\right\}\right] \tag{6.16}$$

$$I_1 = \frac{V_{T2}}{R} + \frac{1}{K'\left(\frac{W}{L}\right)_2 R^2}\left\{\sqrt{2K'\left(\frac{W}{L}\right)_2 R(IR - V_{T2}) + 1} - 1\right\} \tag{6.17}$$

The loop gain can be given as

$$|LG| = g_{m2}R \tag{6.18}$$

And, the effective transconductance can be expressed as

$$g_{m,eff} = (1 + |LG|)g_{m1} \tag{6.19}$$

It can be seen that increase in I_1 will cause an increase in g_{m1}, but a consequent decrease in I_2 will cause a decrease in g_{m2}. Thus, there will be a particular pair of values of I_1 and I_2 for which the loop gain and the effective transconductance will be maximum. It is desirable to find the distribution of I_1 and I_2 for the maximum loop gain, but it might not be suitable to meet the bandwidth performance, which is discussed next.

The location of the second pole can be given by

$$p_2 = -\frac{1}{RC_{gs2}} \tag{6.20}$$

In this design, the product of the loop gain and the second pole can be given by

$$\left|(LG)p_2\right| \cong \frac{g_{m2}}{C_{gs2}} \cong f_T \tag{6.21}$$

Again, in this design, there exists a trade off in the boosting of the effective transconductance and the location of the second pole. If the location of the second pole has to be kept large, then the loop gain has to be sacrificed. This will be an important aspect in the design of this source follower if it were to be integrated with the op amp.

Next, the design of the circuit in Figure 6.3 is presented. In this design, the location of the second pole is given importance over the loop gain. First, let us assume that the channel lengths of the devices are already fixed. Assuming a particular value for R, and the location of the second pole, W2 can be determined from the following equation.

$$W_2 = \frac{1}{R\left(0.67C_{OX}\left|p_2\right|L_2\right)} \tag{6.22}$$

Now, with R and W2 known, we can determine the currents I_1 and I_2 from Equations (6.16) and (6.17). It should be checked that for the obtained value of I_1, the voltage drop across the resistor should be large enough to turn on M2 appreciably. Otherwise, a different value of R has to be selected, and W2 has to be found accordingly.

Next, the loop gain and the effective transconductance can be calculated using Equations (6.18) and (6.19). Note that in this design flow, the stress is not

on maximizing the effective transconductance but to keep the second pole further away. The circuit shown in Figure 6.3 was fabricated in a 0.18 μm CMOS process to verify the proposed concept. The circuit elements are shown in Table 6.3, where the load consisted of a 50 Ω resistance in parallel with a 10 pF capacitance. The simulation and measurement results for this circuit are shown in Table 6.4

Table 6.3. Components values of elements in the modified source follower

Component	**Value**
I (mA)	1.5
M1	125/0.18
M2	40/0.18
R	1 KΩ

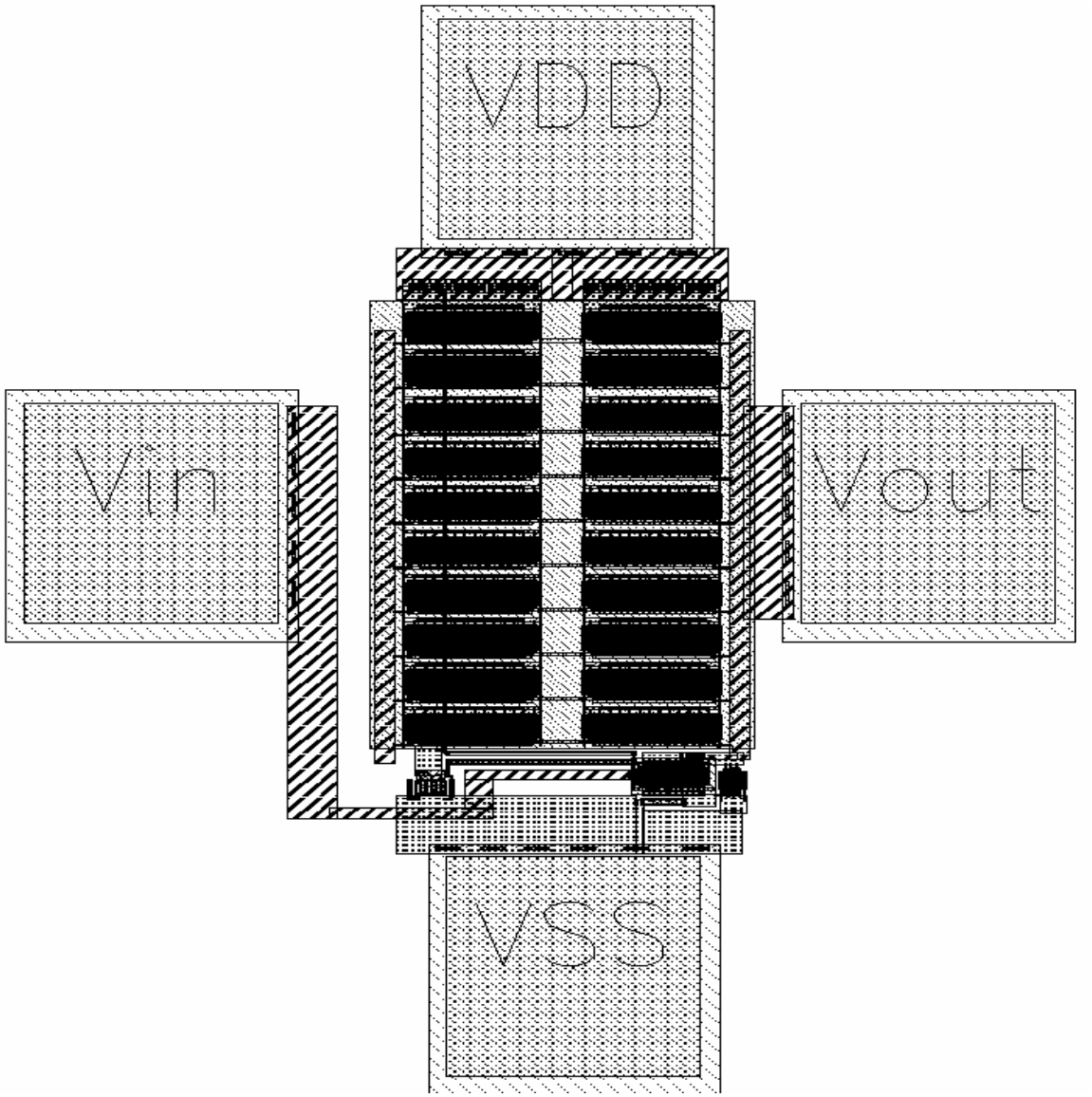


Figure 6.4. Layout of the modified source follower

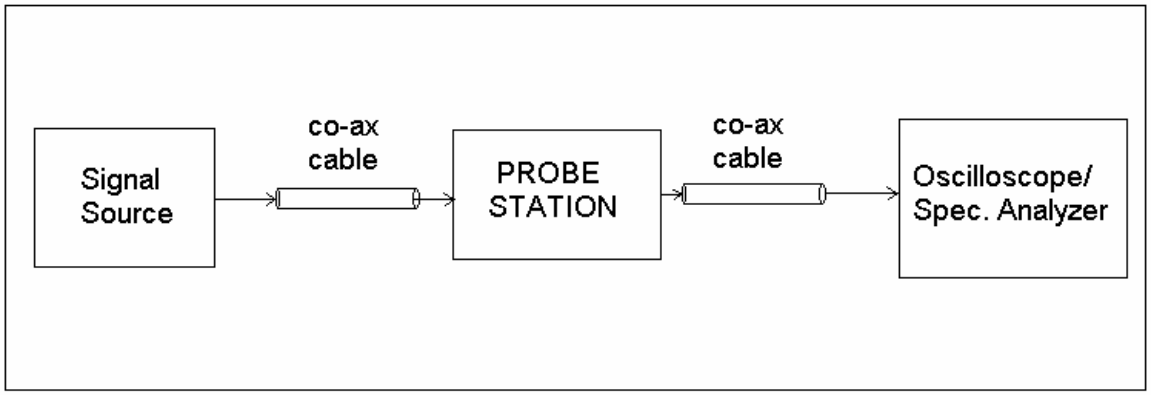


Figure 6.5. Measurement setup of the probe station

The measurement setup of the probe station was similar to the one described in Figure 4.26, and it is redrawn in Figure 6.5. Various equipments used during testing are listed in Table 4.15.

A comparison of the simulated and measured performance of the modified source follower in Figure 6.3 is presented in Table 6.4. The transconductance of a square law MOS device can be given as

$$g_m = \sqrt{2K'\left(\frac{W}{L}\right)I} \tag{6.23}$$

Equation (6.23) will be an approximation for short channel devices. As shown in Table 6.3, if we assumed that in a single transistor source follower, the input device of size 125/0.18 carried a bias current of 1.5 mA, then in the 0.18 μm CMOS process, its g_m will be approximately equal to 10 mS. From Table 6.4, it can be seen that the effective transconductance was improved by a factor of 5 and 3 in simulation and measurement respectively. This was achieved due to g_m boosting. In a single transistor source follower, in order to achieve g_m in the

order of the modified source follower, both current and input device size has to be increased. The boost in the g_m improved the measured gain to about 0.6 V/V for a 50 Ω output load resistance.

The bandwidth could not be measured because the losses in the co-axial cables were significant. The bandwidth of these co-axial cables with a 50 Ω resistance was measured to be almost 15 MHz. These losses could have been estimated using two independent measurements: one with the DUT (device under test) and the other without the DUT, but in both the cases, the input and the output needed to be terminated with a 50 Ω resistance. In the measurement setup, while making measurements in presence of the DUT, the input impedance of the source follower was not 50 Ω (due to high impedance gate of M1), where as in absence of the DUT, the input impedance was about 50 Ω. This caused different power transfers from the input to the output as a function of the frequency in both the cases, which prevented the extraction of the losses in the co-axial cables. The time-domain input and output responses of the modified source follower are shown in Figure 6.6. Even though the bandwidth could not be measured, the simulated frequency response is presented in Figure 6.7.

Table 6.4. Performance of the modified source follower

Specification	Simulated value	Measured value
Effective g_m	50 mS	30 mS
A_V	0.7	0.6
p_1	1.1 GHz	-
p_2	1.2 GHz	-
HD2 (45 mVp-p, 50 Ω)	28 dB	25 dB

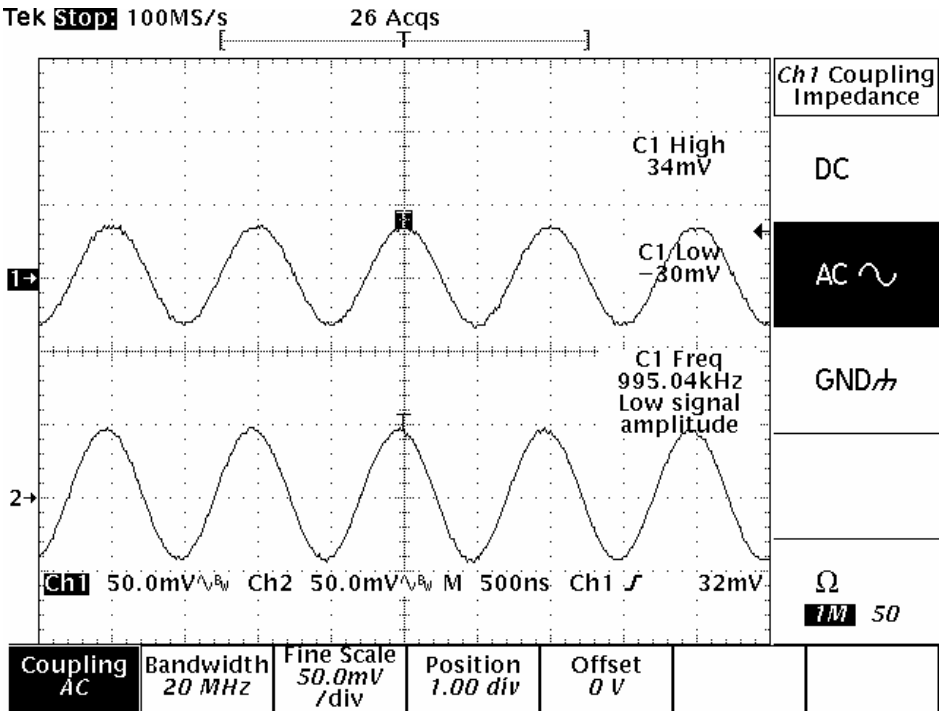


Figure 6.6. Time domain input (Ch2) and output (Ch1) waveforms of the modified source follower

In Figure 6.6, the small-signal gain of the source follower is about 0.6 V/V for a 50 Ω output load. The gain was improved because the effective transconductance of the modified source follower was boosted by a factor of almost 3 compared to a single transistor source follower.

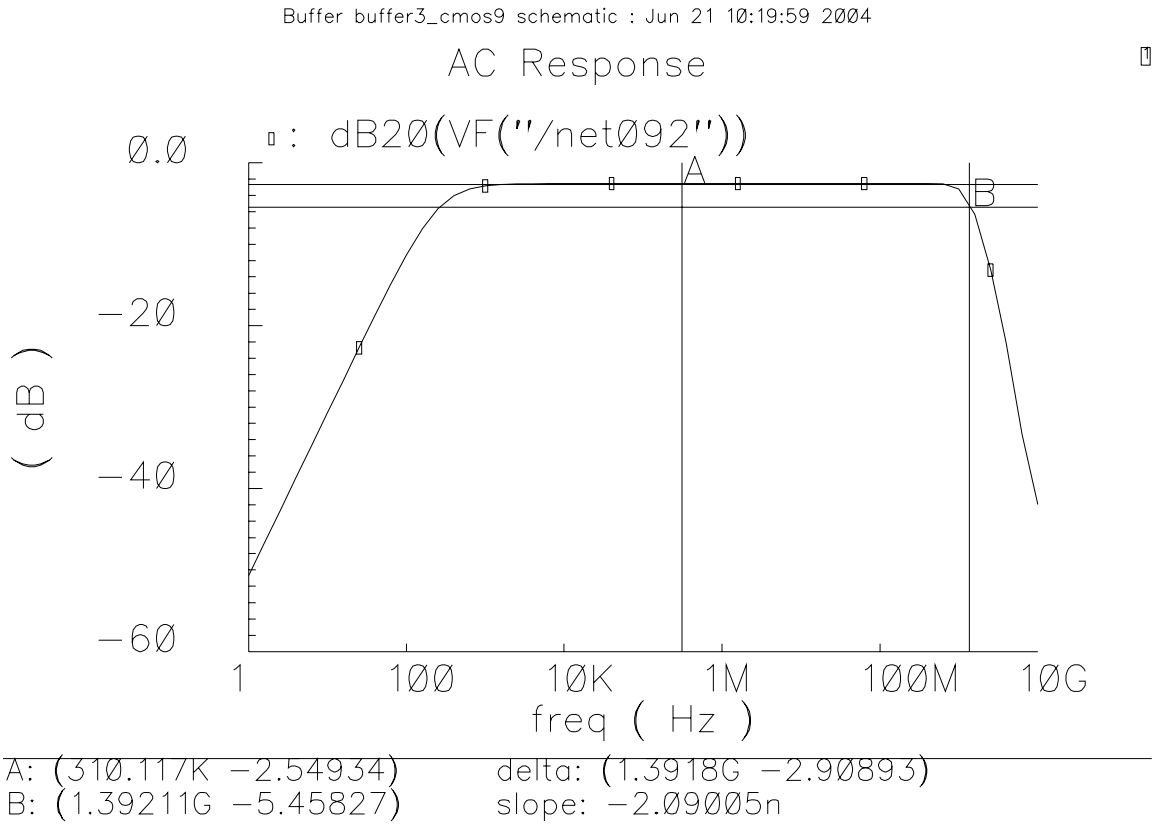


Figure 6.7. Simulated small-signal BW of the modified source follower

In Figure 6.7, the low frequency roll off is due to the dc blocking capacitors at the output. The simulated mid-band gain was 0.7 V/V, but the actual measured gain was only 0.6 V/V. This was probably caused by a smaller loop gain than designed. The simulated BW was about 1.1 GHz, and the location of the second pole was about 1.2 GHz.

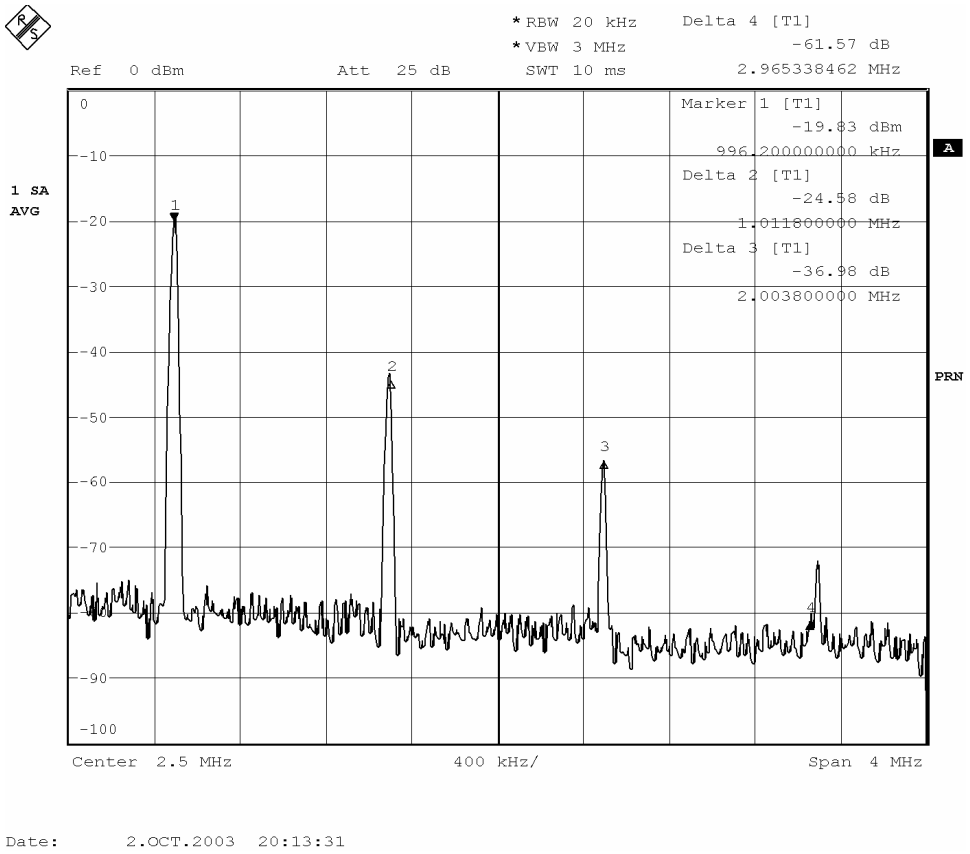


Figure 6.8. HD2 of the modified source follower

The HD2 for a 45 mVp-p output is about 25 dB. The distortion performance of the modified source follower is poor due to the following reasons:

1. Small-signal gain is less due to driving 50 Ω output load resistance.
2. Small channel length devices have poor r_{ds}, which degrade the linear gain.
3. The voltage drop across the resistor tends to decrease V_{ds1}, which pushes M1 out of saturation and degrades the linear gain

6.3 Current Feedback g_m Boosted Push-Pull Source Follower

The source followers presented in Figures 6.1 and 6.3 are not suitable for large input signal swing. While integrating such a buffer with an op amp, the

outputs of the op amp will have large-signal swing, and a push-pull buffer with complementary input stages will be needed to handle the large-signal input. Such a buffer is shown in Figure 6.9. It is a two-stage, push-pull source follower, whose second stage uses current feedback to boost the effective transconductance.

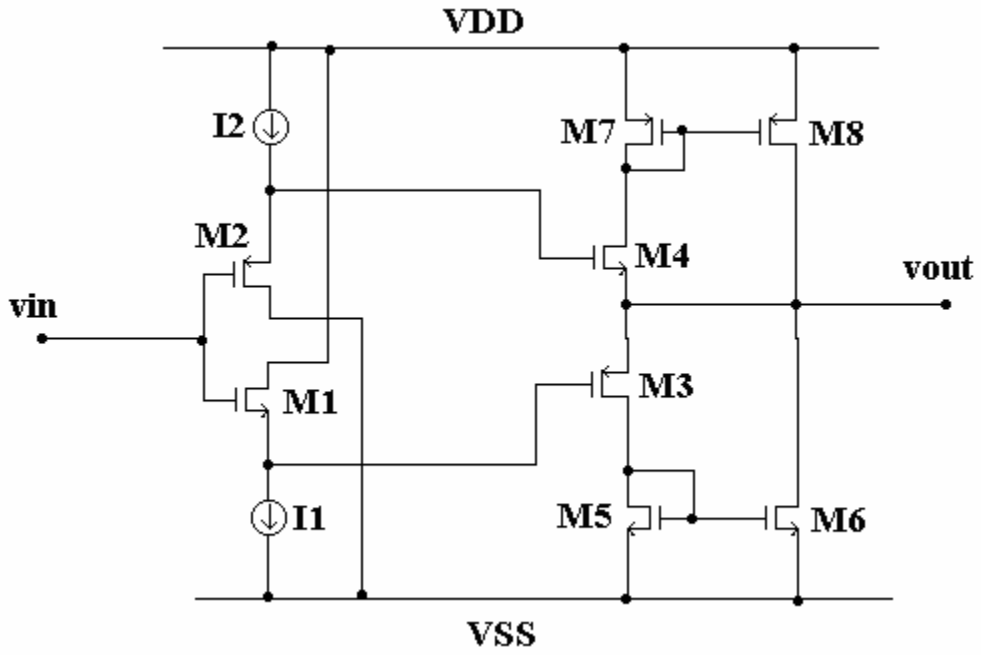


Figure 6.9. Modified push-pull source follower

In Figure 6.9, it is intended that the quiescent operating voltages at the input and the output should be the same. This can be achieved by careful design of M1 through M4 such that

$$V_{gs1} = V_{gs3} \text{ and } V_{gs2} = V_{gs4} \tag{6.24}$$

In Figure 6.9, the first stage is a simple source follower stage with complementary devices. The second stage is a g_m boosted stage, which works on the same

principle as the circuit shown in Figure 6.1. The overall two-stage source follower is effectively a 3 pole system, all of which should be large enough not to appreciably affect the phase margin of the op amp. The overall gain of the source follower is the product of the gains of each of the two stages.

The simulation results for the circuit in Figure 6.9 in the 0.18 μm CMOS process are presented next. The output load consisted of a 50 Ω resistor in parallel with a 10 pF capacitor.

Table 6.5. Simulated performance of the push-pull source follower

Specification	**Value**
VDD	1.8
Total bias current	3 mA
Gain	0.66
BW	900 MHz
Linear input range (for gain > 0.5)	0.5 V – 1 V
HD2 (50 mVp-p, 50 Ω)	39 dB

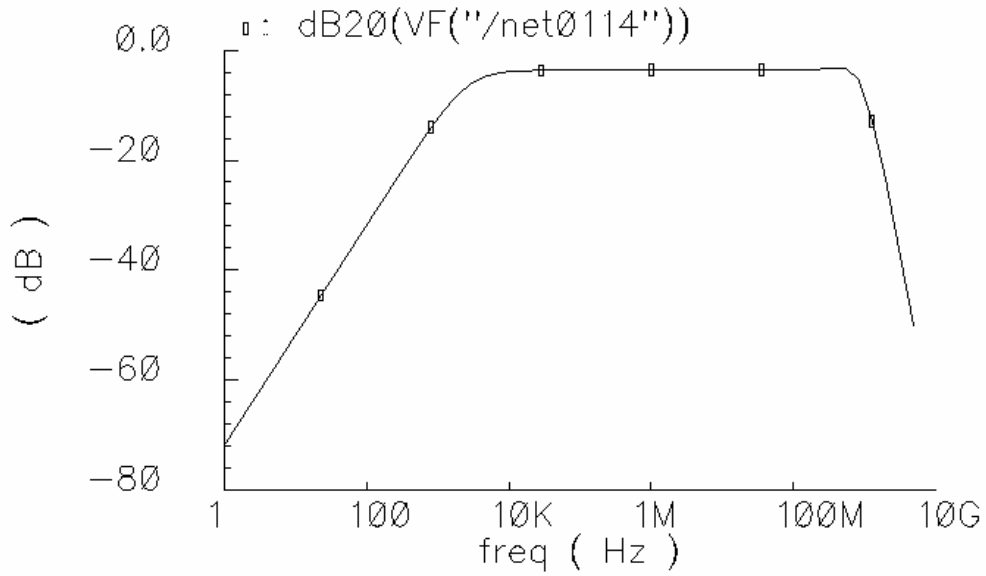


Figure 6.10. Small-signal gain and bandwidth of the push-pull source follower

In Figure 6.10, the small-signal gain was about 0.62 V/V, and the bandwidth was about 900 MHz. The low-frequency roll off is due to the dc blocking capacitors at the output. The gain was poor because it is given by the product of the gain of the two source follower stages; the gain of each stage was less that 0.85 due to bulk effects of the NMOS devices. The simulated time-domain response is shown next in Figure 6.11. The applied input was a 10 MHz, 1Vp-p sine wave. The output suffered from larger saturation effects for positive input swings than the negative input swings.

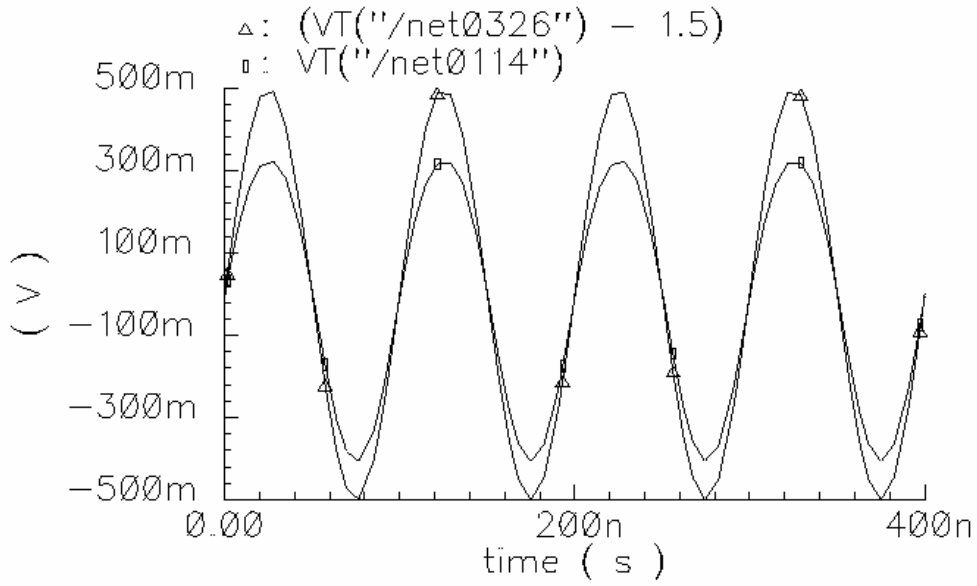


Figure 6.11. Large-signal time domain input and output signals for a purely capacitive output load

Next, the distortion performance of the buffer was simulated using a 1 Vp-p sinusoidal wave, and as shown in Figure 6.12, HD2 was found to be 25 dB for this large-signal input.

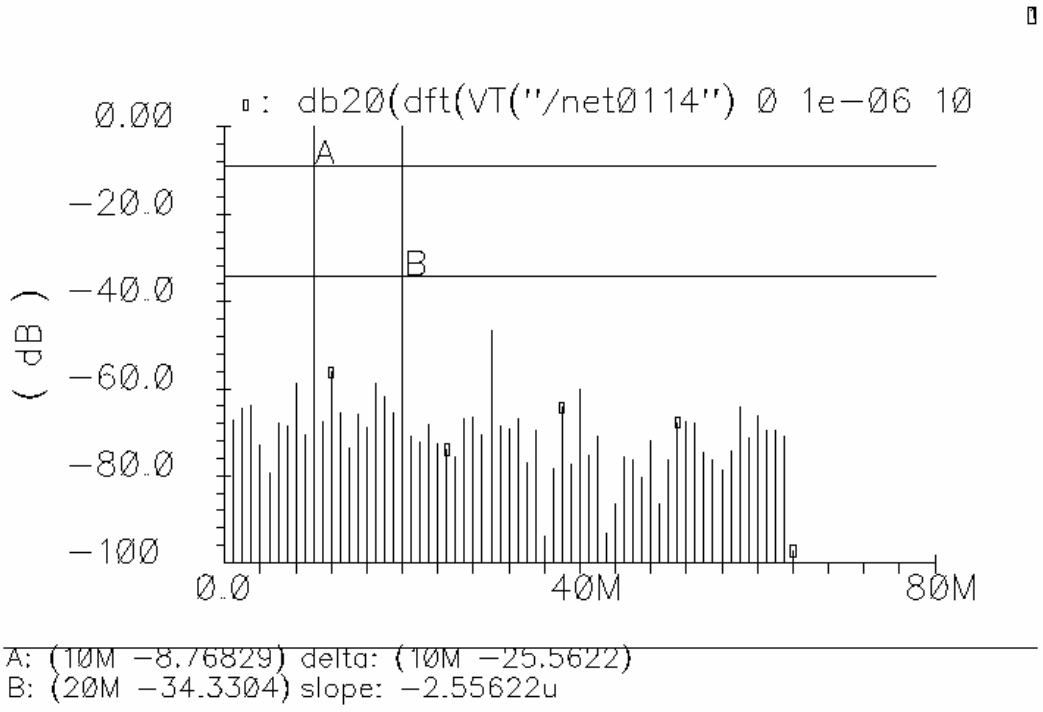


Figure 6.12. Harmonic distortion of the push-pull source follower for a purely capacitive output load and 1 Vp-p sinusoidal input.

In case of driving a 50 Ω output load, the distortion will also be poor for small-signal inputs, and it is shown in Figure 6.13 for a 100 mVp-p sinusoidal input, which gave the HD2 as 39 dB for a 50 Ω load.

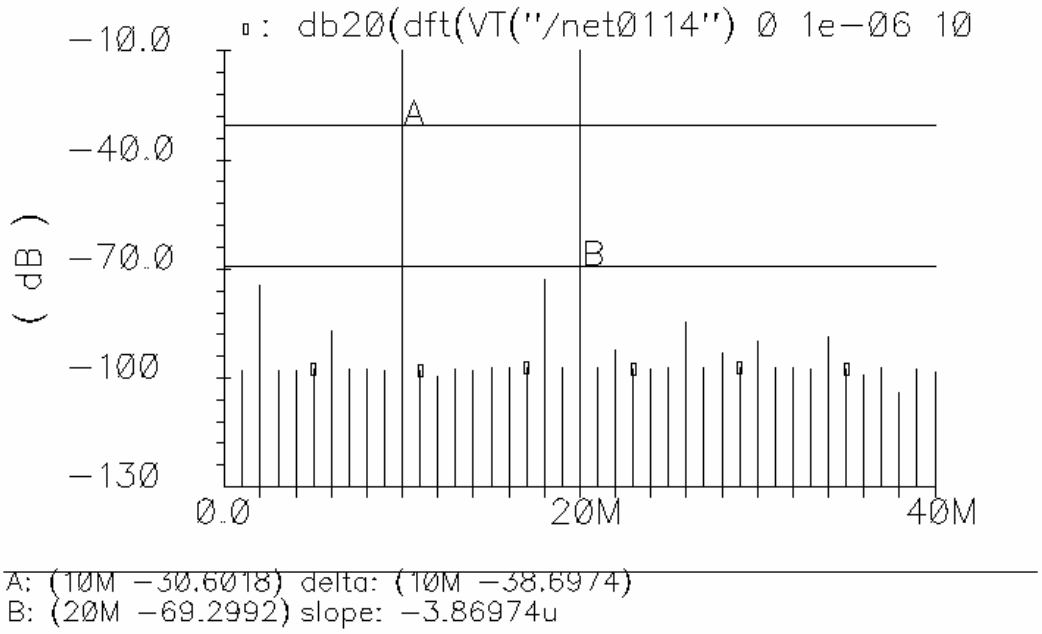


Figure 6.13. Harmonic distortion of the push-pull source follower for 50 Ω output load and 100 mVp-p sinusoidal input.

In the next section, the buffered version of the op amp, *OP*2, is described.

6.4 Buffered *OP2*

The op amp, *OP2*, developed in the previous chapters, needs to be buffered because during testing, the output load capacitance was 20 – 50 times larger than its maximum designed value. In this op amp, all minimum feature-size channel length devices were used, and an adaptive PMOS bulk drive scheme was

used to generate the bias currents. The overall buffered op amp architecture is shown in Figure 6.14, where the last stage is implemented by two push-pull source followers as shown in Figure 6.9.

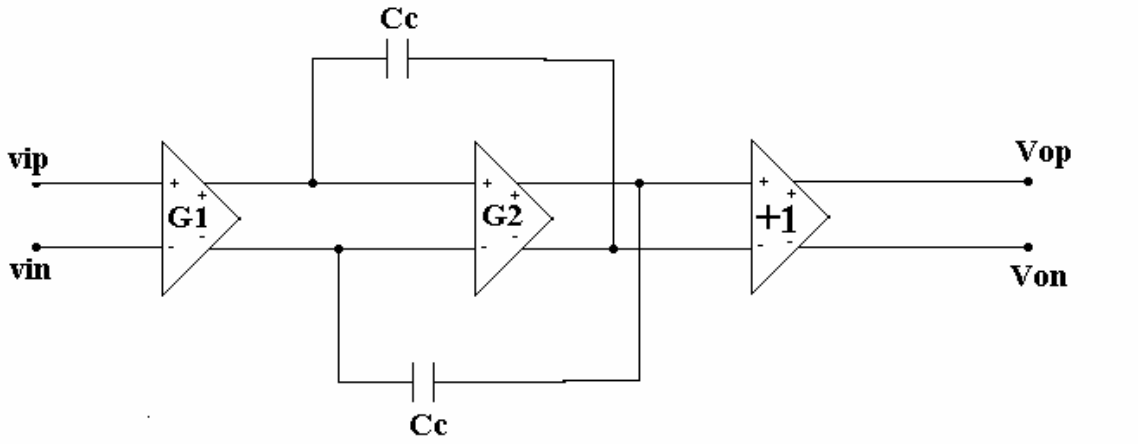


Figure 6.14. Buffered *OP2*

In Figure 6.14, due to the presence of the output source follower, the ICMR range of the overall op amp will be slightly reduced.

6.4.1 Simulation Results of Buffered *OP2*

This op amp was simulated in the 0.25 μm CMOS process and the 0.18 μm CMOS process, and their simulated performance is compared in Table 6.6. During measurements, the oscilloscope probes caused a loading of 2.5 pF, and the total output load capacitance was 10 pF.

Table 6.6. Comparison of the simulated performance of buffered *OP2* in the 0.25 μm and the 0.18 μm CMOS processes

Performance specification	**Simulated value**	
	0.25 μm CMOS	0.18 μm CMOS
Vdd	2 V	1.5 V
A_v	67 dB	62 dB
UGBW (single-ended CL= 10 pF)	24 MHz	19 MHz
Phase margin	71 deg	65 deg
Slew rate (single-ended CL= 10 pF)	14 $V / \mu s$	10 $V / \mu s$
ICMR	0.64 – 1.395 V	0.52 – 1.01 V
PSRR (at dc)	68 dB	64 dB
Idd (op amp) Idd (source follower)	820 μA 3.3 mA	520 μA 3.3 mA

The above comparison shows that insertion of the output source follower did not affect the overall performance of the op amp considerably, and their gain, and phase margin remained relatively constant in both the processes. This op amp was fabricated in the 0.25 μm CMOS process, and the measured results are presented next. It was not fabricated in the 0.18 μm CMOS process because the un-buffered version of this op amp had already failed to operate satisfactorily due to uncontrolled PMOS bulk drive.

6.4.2 Measurement Results of Buffered *OP2*

The layout of buffered *OP2* is shown in Figure 6.15.

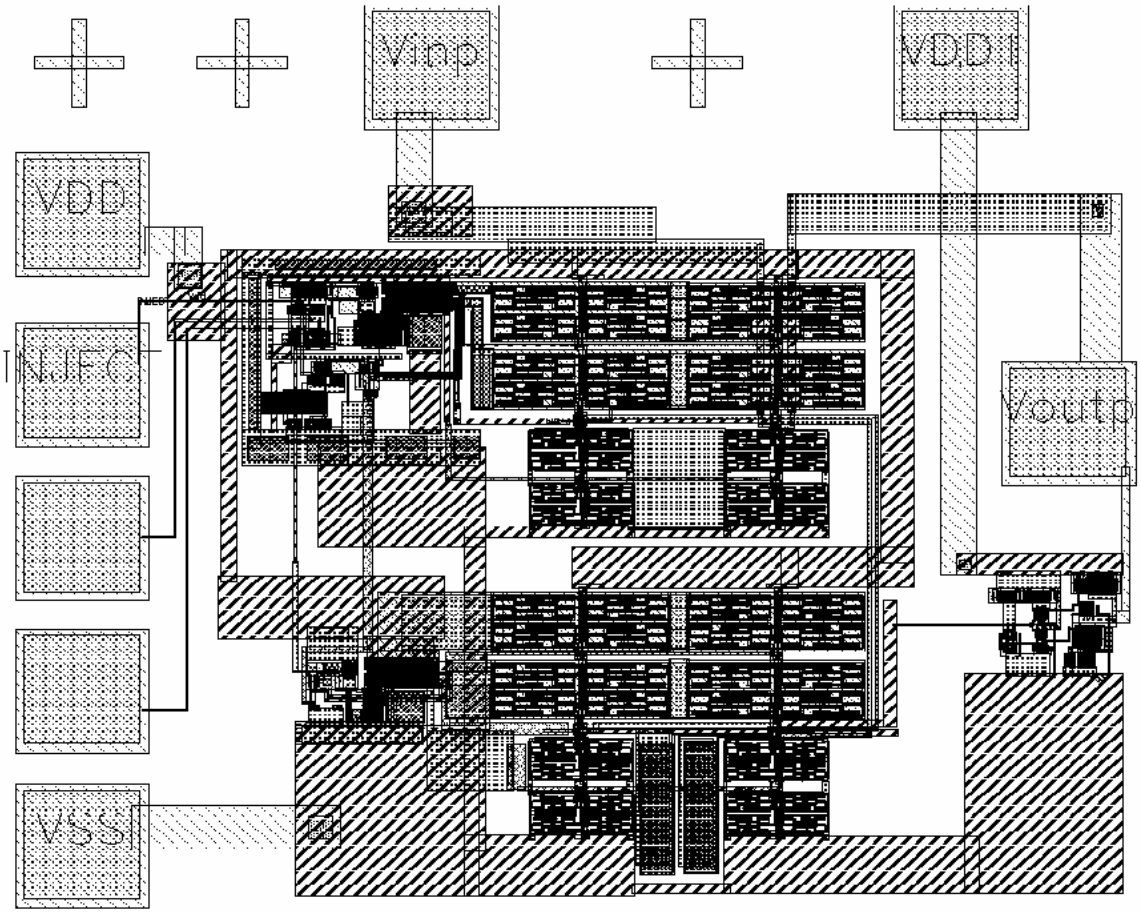


Figure 6.15. Layout of buffered *OP2* in both the CMOS processes

During processing in the 0.25 μm CMOS process, there was an unexpected update in the fabrication, but the updated device models were not available at the time of designing the circuit. It was later found through measurements that the fabricated value of a resistance was almost 50% more than the simulated value. This effected the generation of the bias current in the bias current generation circuit shown in Figure 3.11 considerably. It also effected the generation of the limiting current for the PMOS bulk drive. These currents were smaller than the simulated value. The total measured bias current in the two gain stages was measured to be almost 25% of the simulated value.

Smaller limiting current for the bulk drive affected the bulk drive of the PMOS devices in the second gain stage of the op amp. During the design, it was intended that the bias current in the second gain stage should be 5 times the current in the first gain stage in order to achieve a good phase margin. This 5 times larger bias current in the second gain stage was generated by forward biasing of the PMOS bulk diodes such that their threshold voltage could be reduced. After fabrication, since the forward biased PMOS bulk diode currents were smaller, the extent to which these PMOS bulk diodes could be forward biased was limited, and overall this resulted in a much smaller bias current in the second gain stage. This degraded the phase margin, and reduced bias currents also affected the large-signal slewing capability of the op amp. The measured performance of this op amp is summarized in Table 6.7.

Table 6.7. Comparison of the simulated and measured performance of the buffered *OP2* in the 0.25 μm CMOS process

SPECIFICATIONS	**Simulated value**	**Measured value**
Channel length	0.25 μm	0.25 μm
VDD (V)	2	2
IDD (mA)	**0.82 (op amp)** **3.3 (source follower)**	**0.25 (op amp)** **2 (source follower)**
Vos (mV)	-	4
Av (dB)	67	-
UGBW (MHz) (CL=10 pF)	24	-
PM (deg) (CL=10 pF)	**71**	**40**
SR (V/us) (CL=10 pF)	**14**	**4**
ICMR	0.64 V – 1.395 V	0.592 V – 1.345 V
PSRR (at dc)	68 dB	40 dB for 100 mV change in VDD

Due to reduced bias current in the second gain stage, the phase margin was poor, and it also resulted in poor slewing capability of the overall op amp. The UGBW frequency could not be measured satisfactorily due to losses in the co-axial cables.

The input offset voltage of buffered *OP2* in the 0.25 μm CMOS process is presented next. Even though the bias currents were much smaller, it still had small input offset voltage.

Table 6.8. Input offset voltage of buffered *OP2* with varying input common-mode voltage in the 0.25 μm CMOS process

Vicm (V)	**Vos (mV)**
0.6	12
0.7	12
0.8	8
0.9	4
1.0	**4**
1.1	4
1.2	4
1.25	1
1.3	-7

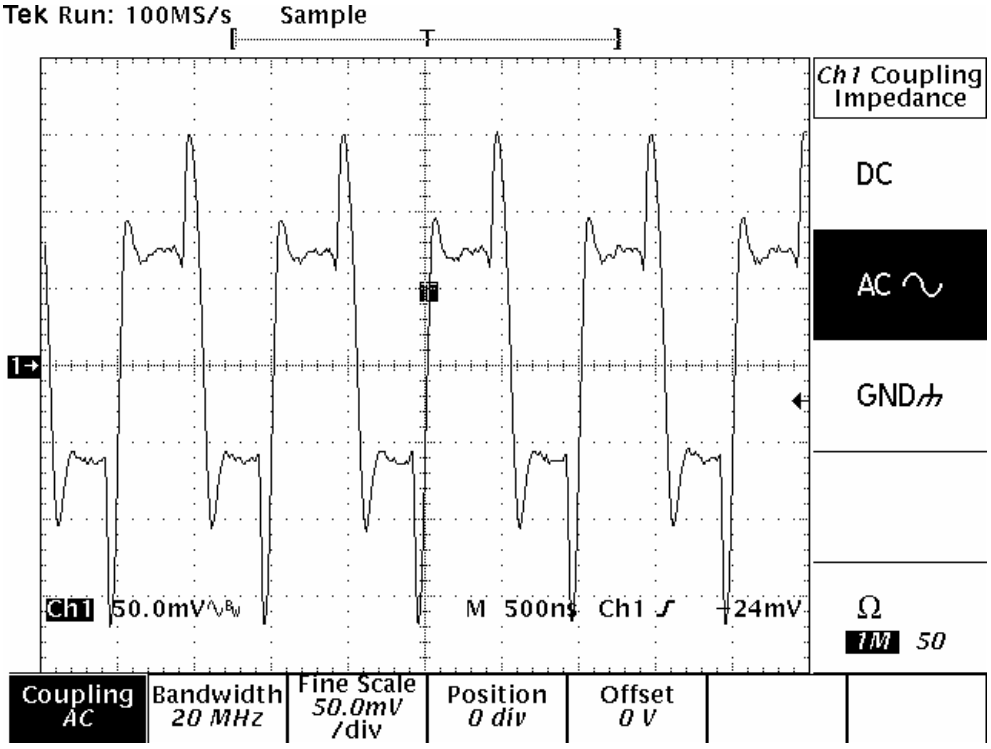


Figure 6.16. Small-signal step response of buffered *OP2* in the 0.25 μm CMOS process

The small-signal positive and negative overshoots of the op amp were about 20% and 33% respectively. This corresponded to a worst-case phase margin of about 40 degrees. Next, in Figure 6.17, the large-signal slewing of the op amp is shown.

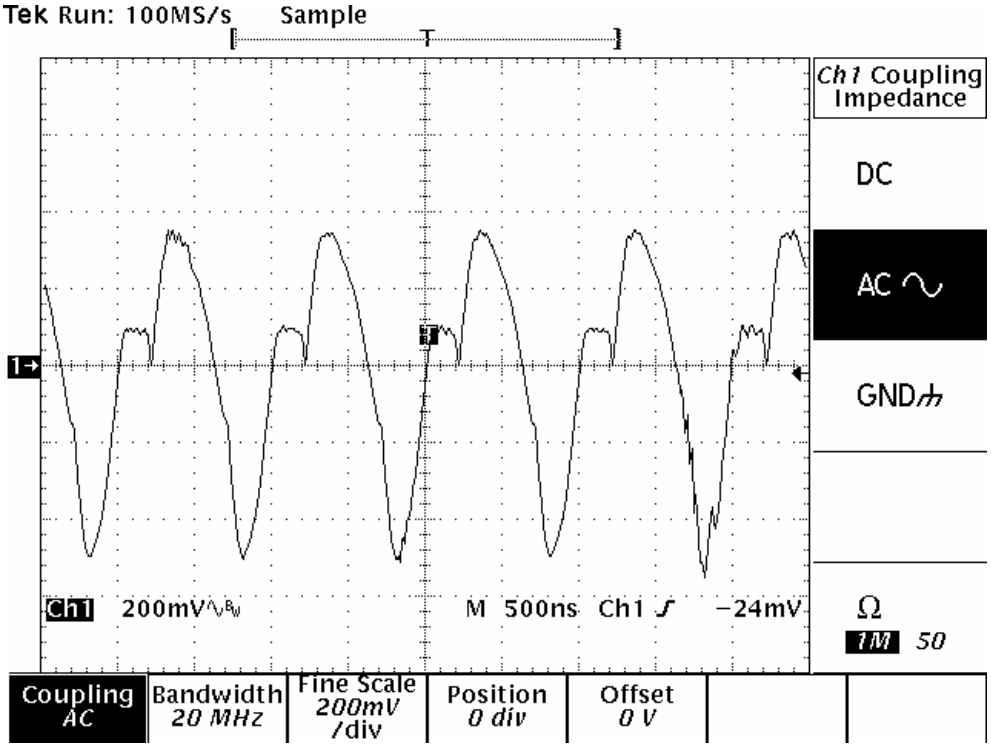


Figure 6.17. Large-signal slew of the buffered *OP2* in the 0.25 μm CMOS process

The large-signal SR was about 4 V/us. It is less than expected because of decrease in the bias currents. Overall, the performance of the buffered *OP2* in the 0.25 μm CMOS process was poor. The update in the fabrication process did not get reflected in the device models during simulation, which effected the biasing of the various stages in the op amp, and the desired performance could not be achieved.

6.5 Buffered *OP3*

The op amp, *OP3*, which was developed in the previous chapter, was buffered at the output using the push-pull source follower shown in Figure 6.9, and the overall op amp is shown in Figure 6.18. In this op amp, the channel lengths of all the devices were kept twice the minimum feature size, and all the bulks of the NMOS and the PMOS devices were reversed biased. In Figure 6.18, two push-pull source followers, as shown in Figure 6.9, were combined to implement the differential output buffer stage.

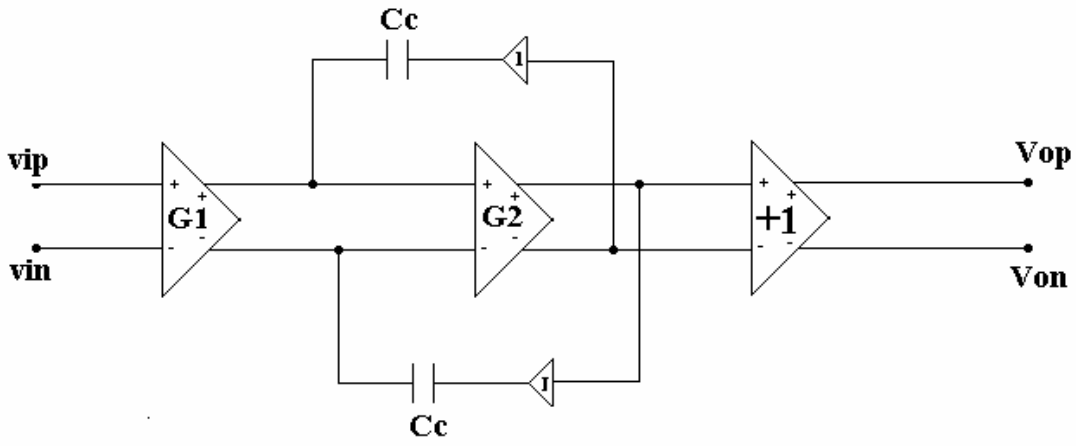


Figure 6.18. Buffered *OP3*

6.5.1 Simulation Results of Buffered *OP3*

This op amp was simulated in the 0.25 μm CMOS process and the 0.18 μm CMOS process, and their simulated performance is compared in Table 6.9.

Table 6.9. Comparison of the simulated performance of buffered *OP3* in the 0.25 μm and the 0.18 μm CMOS processes

Performance specification	**Simulated value**	
	0.25 μm CMOS	**0.18 μm CMOS**
Vdd	2 V	1.5 V
A_v	90 dB	88 dB
UGBW (single-ended CL= 10 pF)	74 MHz	70 MHz
Phase margin	80 deg	74 deg
Slew rate (single-ended CL= 10 pF)	60 V/us	50 V/us
ICMR	0.65 – 1.46 V	0.5 – 1.1 V
PSRR	92 dB	90 dB
Idd (op amp) Idd (source follower)	960 μA 3.3 mA	690 μA 3.3 mA

The above comparison shows that insertion of the output source follower did not affect the overall performance of the op amp considerably, and their gain, phase margin and UGBW frequency remained relatively constant in both the processes.

6.5.2 Measurement Results for Buffered *OP3*

The measured results for the buffered *OP3* in both the CMOS processes are shown next. In these measurements, the op amp was connected in the single-ended unity gain mode. The layout of buffered *OP3* in both the CMOS processes is shown in Figure 6.19. A comparison of the simulated and measured results is shown in Tables 6.10 and 6.11.

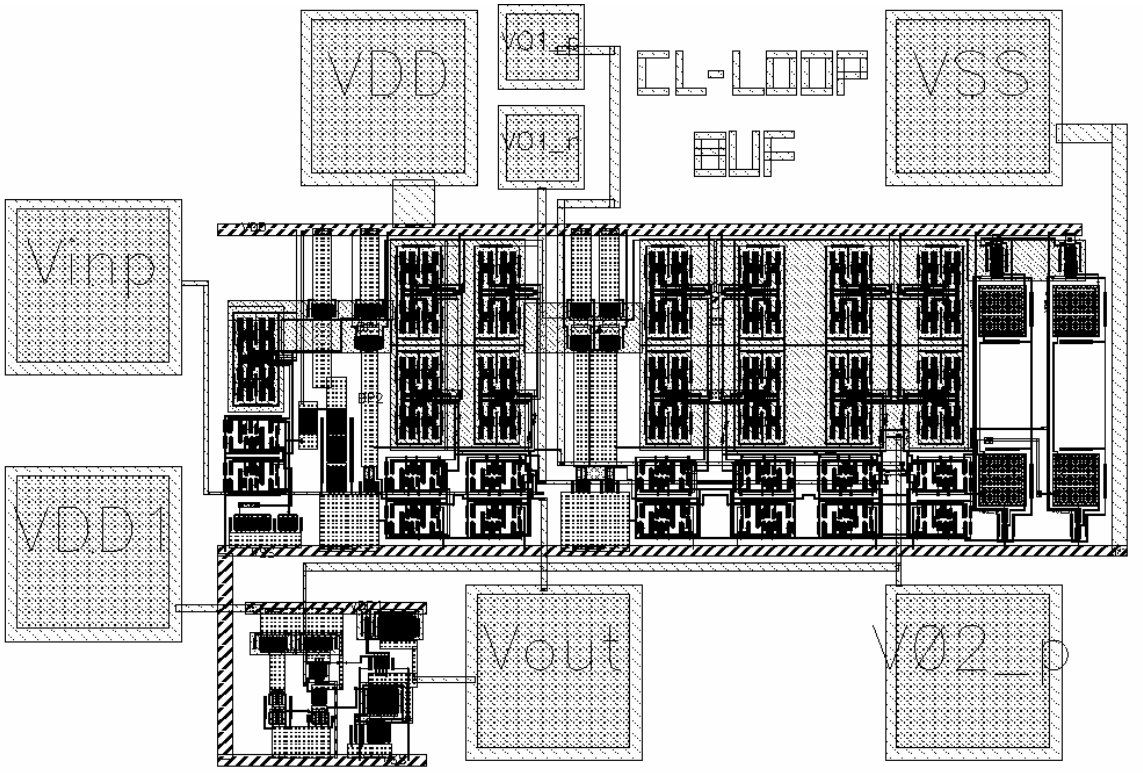


Figure 6.19. Layout of buffered *OP3* in both the CMOS processes

Table 6.10. Simulated and measured performance of the buffered *OP3* in the 0.25 μm CMOS process

SPECIFICATIONS	Simulated value	Measured value
Technology	0.25 μm CMOS	0.25 μm CMOS
Channel length (L)	0.55 μm	0.55 μm
VDD (V)	2	2
IDD (mA)	**0.96 (op amp)** **3.3 (source follower)**	**0.6 (op amp)** **0.88 (source follower)**
Av (dB)	90	-
UGBW (MHz) (CL = 10 pF)	74	-
PM (degrees) (CL = 10 pF)	80	30
SR (V/us) (CL = 10 pF)	60	36
ICMR	0.65 – 1.46 V	0.65 – 1.42 V
PSRR (at dc)	92 dB	46 dB for 200 mV change in VDD

Again, changes in the fabrication process affected the bias currents, which changed the operating point of the output source follower considerably. This resulted in poor phase margin as the poles from the source followers became small. The slew rate was also limited by the slewing characteristics of the source followers. The overall performance of the op amp was degraded by the reduced currents in the source

follower stages. The performance of the op amp in the 0.18 μm CMOS process is presented next, and the same problems during fabrication affected the performance of the op amp.

Table 6.11. Simulated and measured performance of the buffered *OP3* in the 0.18 μm CMOS process

SPECIFICATIONS	**Simulated value**	**Measured value**
Technology	0.18 μm CMOS	0.18 μm CMOS
Channel length (L)	0.35 μm	0.35 μm
VDD (V)	1.5	1.5
IDD (mA)	**0.69 (op amp)** **3.3 (source follower)**	**0.64 (op amp)** **2 (source follower)**
Av (dB)	88	-
UGBW (MHz) (CL = 10 pF)	70	-
PM (degrees) (CL = 10 pF)	74	>70 (CL=2.5pF) < 30 (CL=10pF)
SR (V/us) (CL = 10 pF)	50	10
ICMR	0.5 – 1.1 V	0.52 – 1 V
PSRR (at dc)	90 dB	40 dB for 100 mV change in VDD

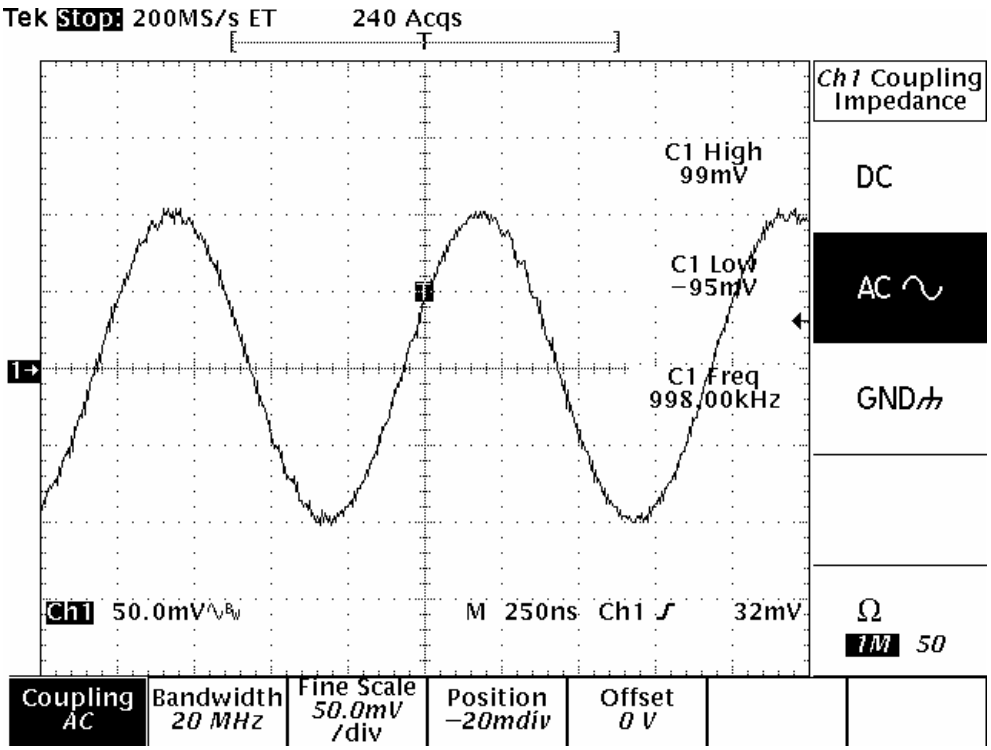


Figure 6.20. Time domain output of buffered *OP3* in unity-gain buffer configuration in the 0.25 μm CMOS process for a CL of 10 pF

In Figure 6.20, a sinusoidal output response is shown for a 1 MHz sinusoidal input. The noise in the output waveform is primarily caused due to the probe setup. The small-signal overshoot for a pulse input is shown next in Figure 6.21.

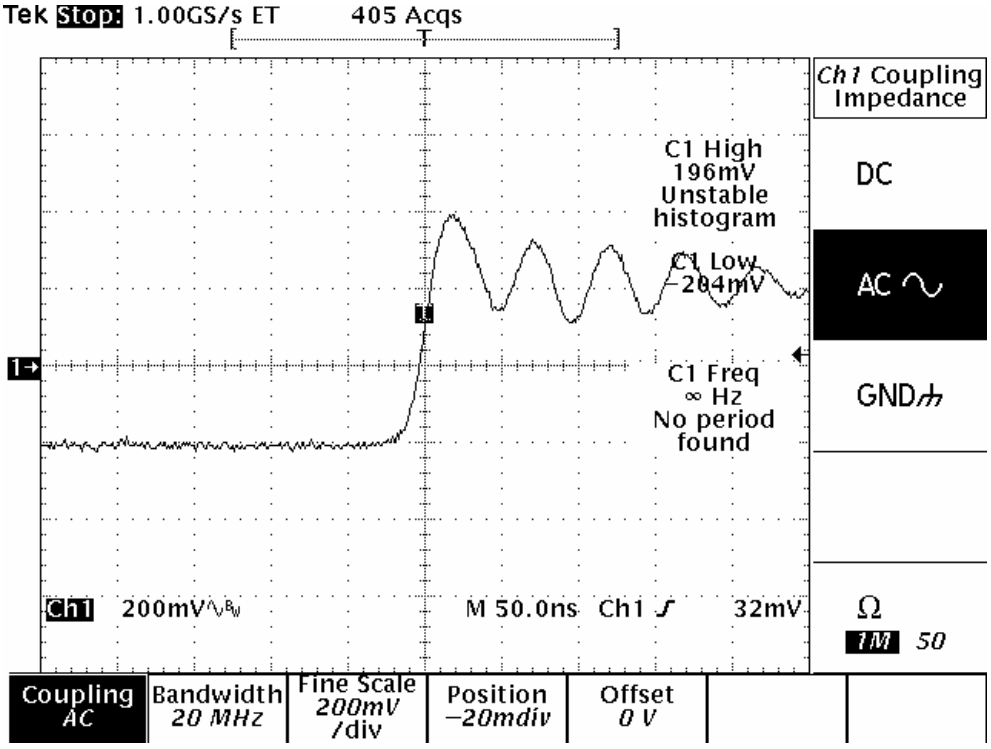


Figure 6.21. Small-signal overshoot of the buffered *OP3* in the 0.25 μm CMOS process

In the 0.25 μm CMOS process, the small-signal overshoot of the op amp was almost 50%. This corresponded to a PM of about 30 degrees, which is poor due to the reduced bias currents in the output source follower. The response of the same op amp in the 0.18 μm CMOS process is shown next.

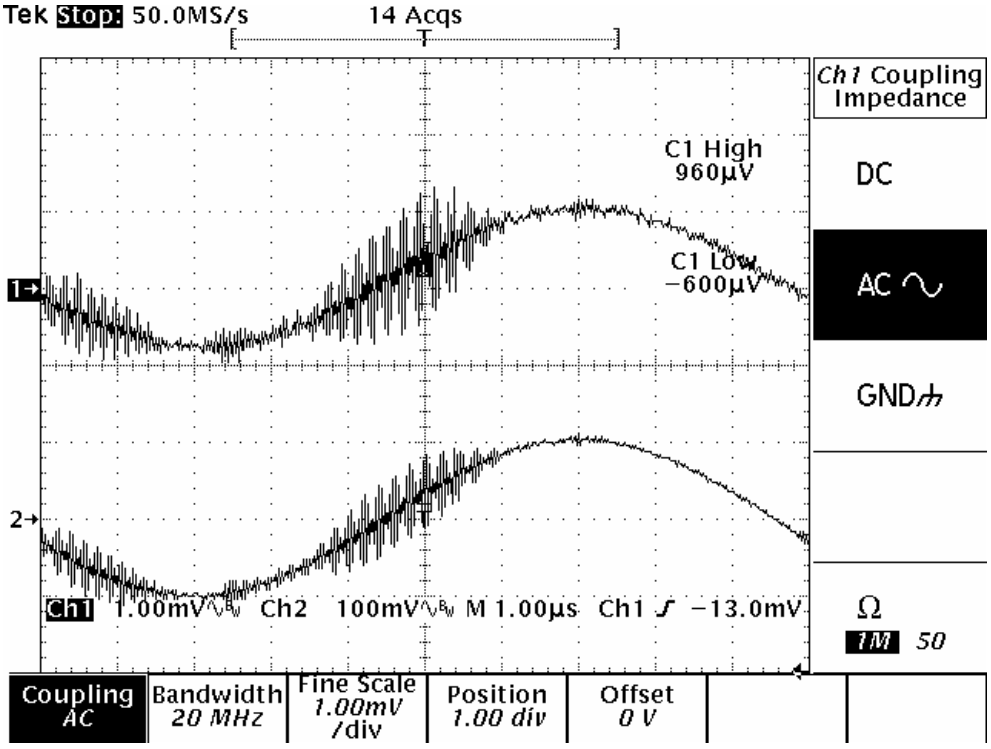


Figure 6.22. Time domain input (Ch2) and output (Ch1) of the buffered *OP3* in the 0.18 μm CMOS process with a 10 pF load capacitance.

In the 0.18 μm CMOS process, it can be seen that for a 10 pF load, the input as well as the output oscillate for lower input voltages. In the 0.25 μm CMOS process, the phase margin of the same op amp was 30 degrees, which got further degraded in the 0.18 μm CMOS process. These oscillations were primarily caused due to the reduced bias currents in the output source followers. When the output loading is reduced from 10 pF to 2.5 pF, the oscillations were greatly reduced, and the plots are shown in Figure 6.23.

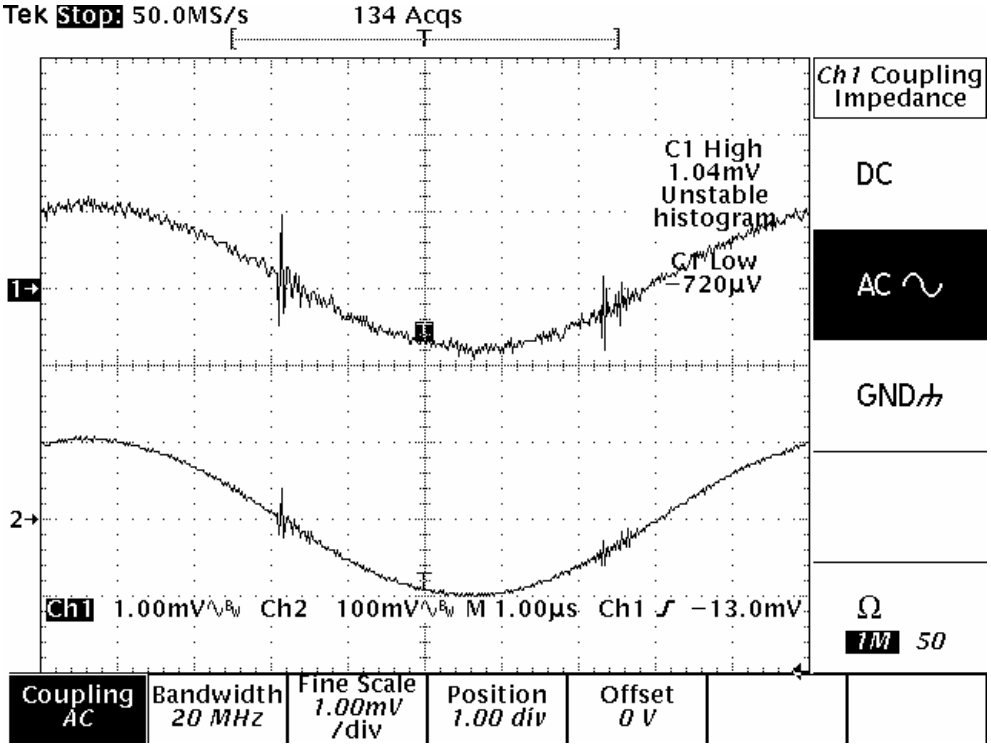


Figure 6.23. Time domain input (Ch2) and output (Ch1) of the buffered *OP3* in the 0.18 μm CMOS process with a 2.5 pF load capacitance

In the 0.18 μm CMOS process, the buffered *OP3* was also excited by pulse waveforms for different output load capacitances, and they are shown in Figures 6.24 and 6.25. In these figures, it can be seen that the output as well as the input waveforms showed oscillations for a 10 pF output capacitance. But, these oscillations were diminished when the output load capacitance was reduced to 2.5 pF.

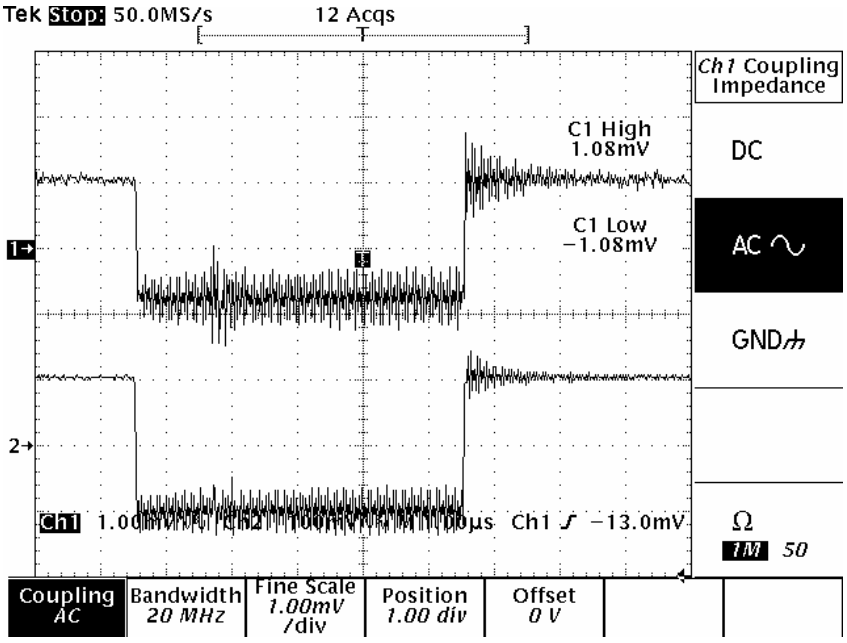


Figure 6.24. Time domain input (Ch2) and output (Ch1) waveforms of the buffered *OP3* in the 0.18 μm CMOS process with 10 pF output capacitance

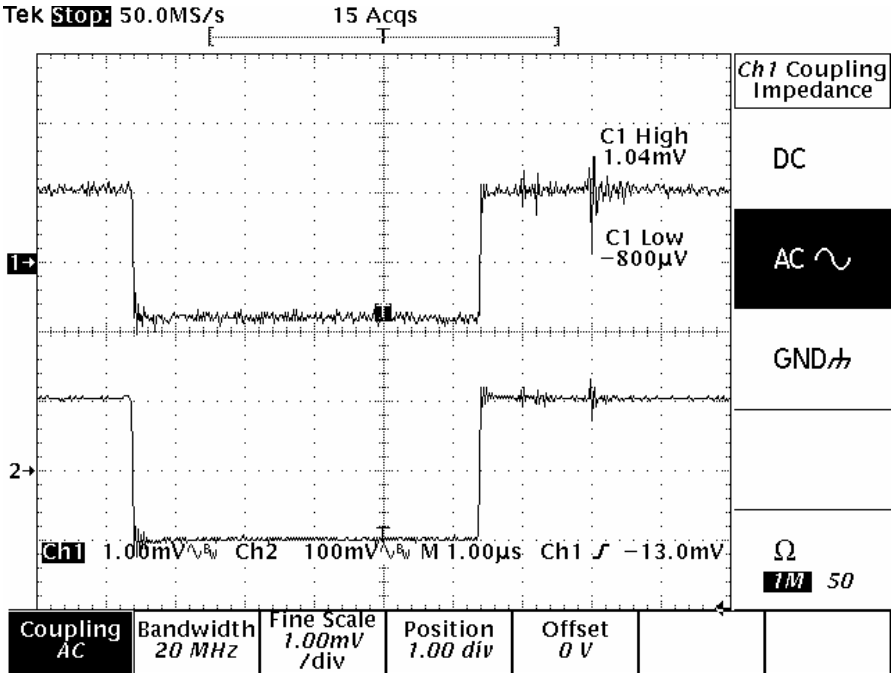


Figure 6.25. Time domain input (Ch2) and output (Ch1) waveforms of the buffered *OP3* in the 0.18 μm CMOS process with 2.5 pF output capacitance

Next, the ICMR was measured with a large-signal pulse input, and it is shown in Figure 6.26.

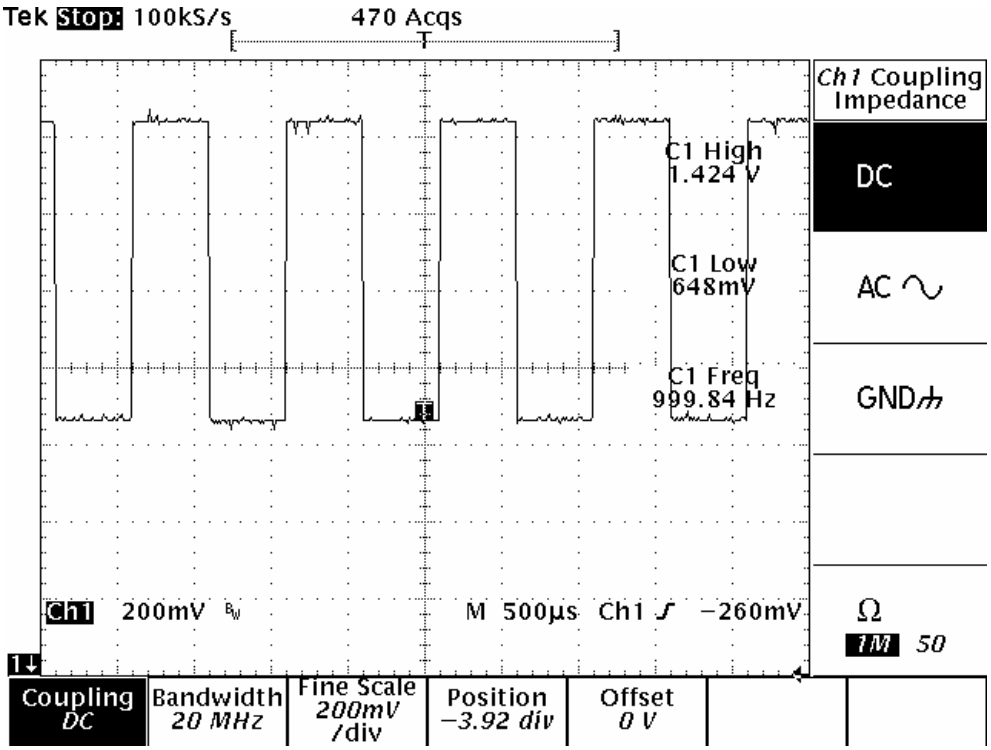


Figure 6.26. ICMR of the buffered *OP3* in the 0.25 μm CMOS process

As shown in Figure 6.26, the ICMR of the buffered *OP3* in the 0.25 μm CMOS process was 0.65 V – 1.42 V, which is slightly less than the un-buffered op amp, because the output source followers limited the large-signal swing of the op amp. It's ICMR in the 0.18 μm CMOS process was 0.52 V – 1 V, and it is shown in Figure 6.27.

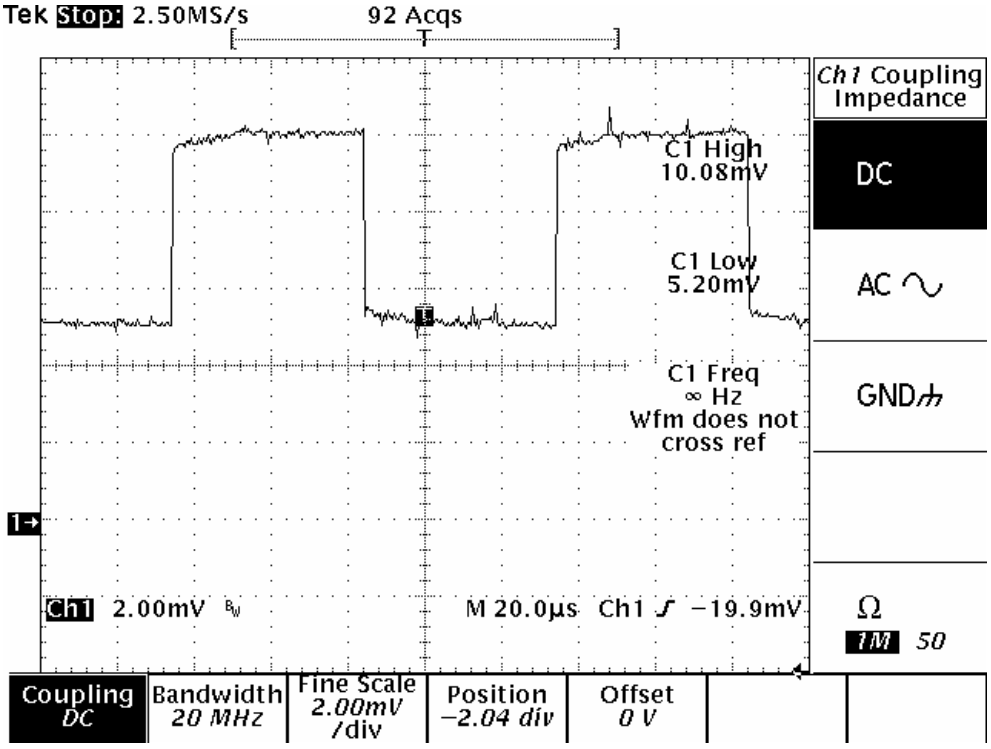


Figure 6.27. ICMR of the buffered *OP3* in the 0.18 μm CMOS process

Next, the slew rate of the op amp was measured in both the CMOS processes, and they are shown next.

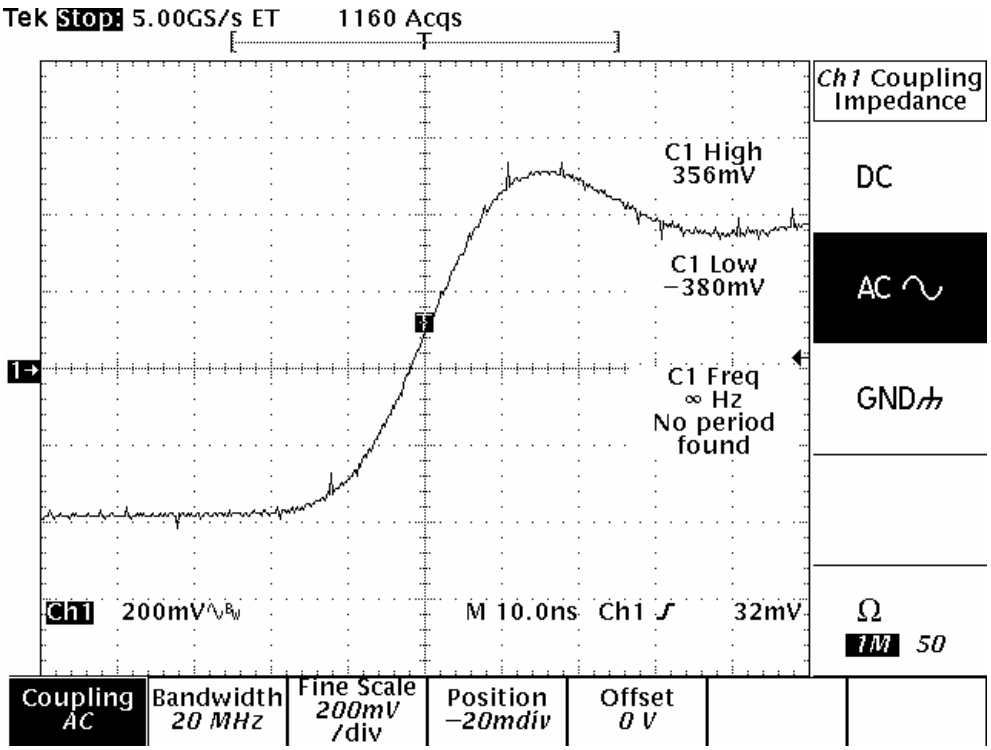


Figure 6.28. Large-signal slew of the buffered *OP3* in the 0.25 μm CMOS process

In the 0.25 μm CMOS process, the buffered *OP3* achieved a slew rate of about 36 V/us, but in the 0.18 μm CMOS process, the slew rate was about 10 V/us, and it is shown in Figure 6.29.

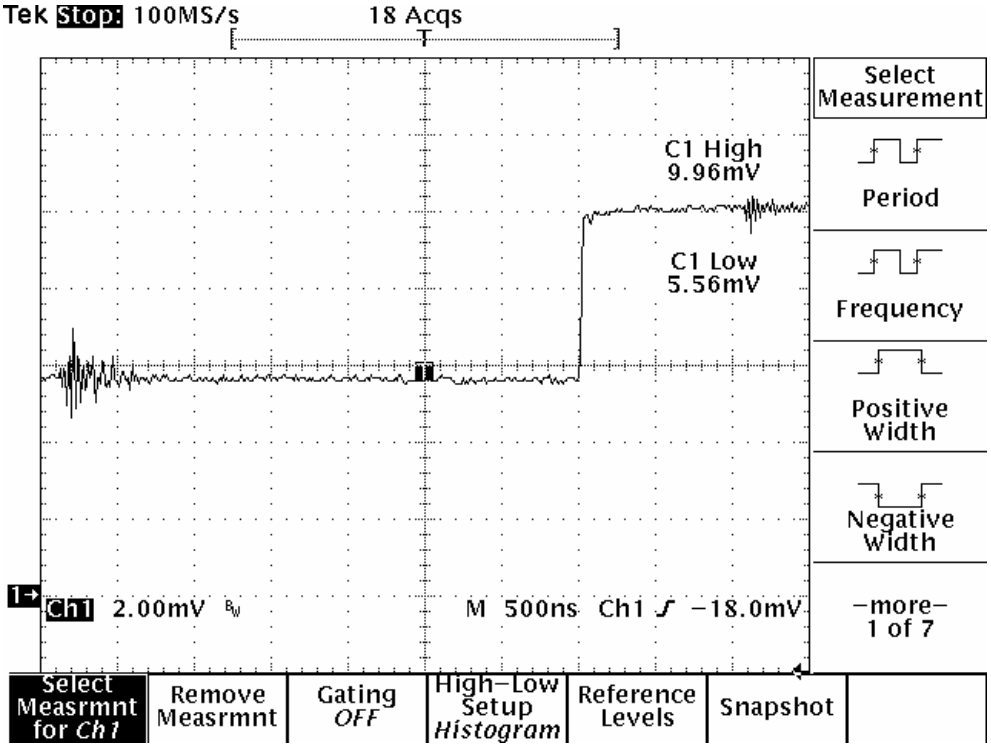


Figure 6.29. Large-signal slew of the buffered *OP3* in the 0.18 μm CMOS process

Finally, the distortion performance was measured in both the CMOS processes, and the plots are shown next. In this design, the harmonic distortion of the output source followers will dominate the overall distortion performance.

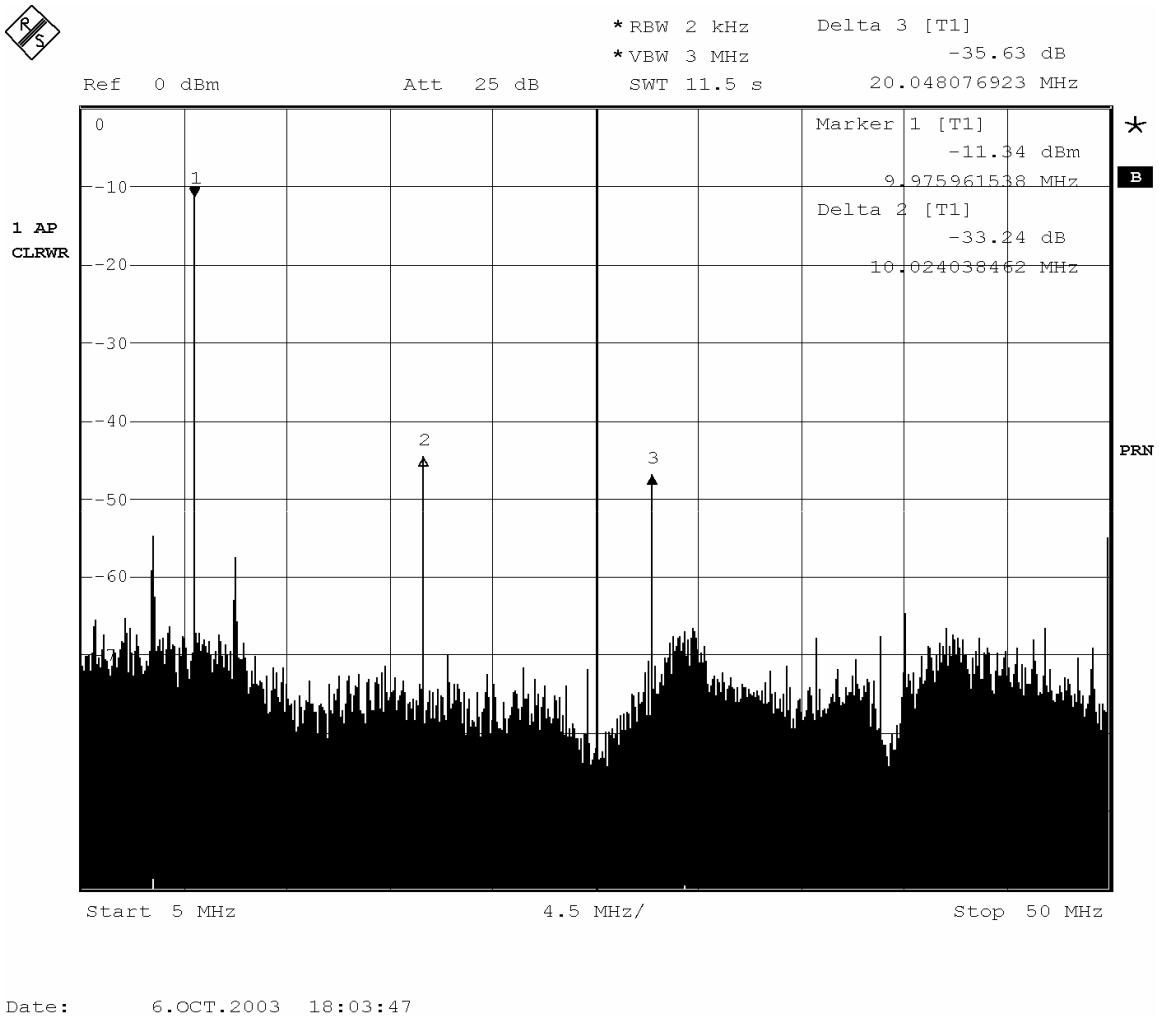


Figure 6.30. Harmonic distortion of the buffered *OP3* in the 0.25 μm CMOS process

In the 0.25 μm CMOS process, the second harmonic distortion (HD2) of the op amp for a 355 mVp-p, 10 MHz sine input was about 33 dB. It is poor primarily due to the output source follower, which carried reduced bias currents. It can be seen that the distortion performance of the buffered op amp is comparable to the source follower by itself. The HD2 in the 0.18 μm CMOS process was about 27 dB, and it is shown in Figure 6.31.

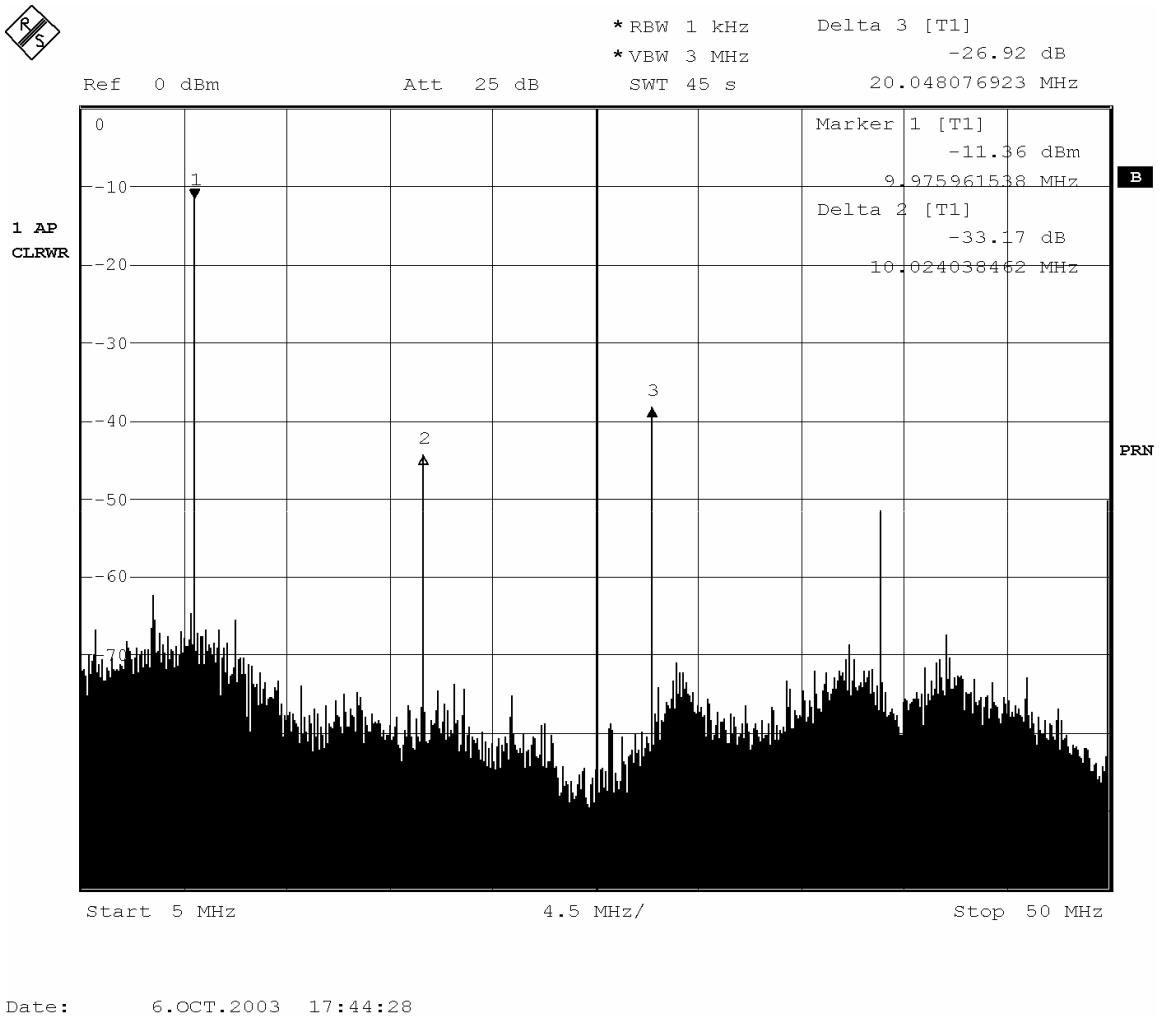


Figure 6.31. Harmonic distortion of the buffered *OP3* in the 0.18 μm CMOS process

6.6 Future Work

In this chapter, the design methodolgy of an op amp with large small-signal gain, constant UGBW frequency and phase margin in different technologies was presented. The performance of the op amp was verified through

simulations, but its measured performance fell short of the simulation results. This was caused by various issues during fabrication and testing phases. With knowledge of these isssues, further fabrication is being carried out, and some of the steps that have been taken are as follows:

1. Further fabrication of the op amps is being done with the knowledge of the updates in the CMOS process. Due to the fabrication timeline, the results from these fabricated circuits will not be included in this thesis.

2. In the previously fabricated chips, internal biasing schemes did not generate proper biasing currents and voltages due to processing changes. The biasing scheme is made external in order to adjust the biasing currents and voltages externally. This will help in verifying the proposed concepts with negligible effect of biasing on the circuit performance.

3. More insight into different nodes of the op amps is made available by routing them to external pads. Some nodes could be sensitive to large capacitive loading of the pads; thus, digitally controlled transmission gates have been used in series with these routes to the pads.

4. The op amps will be packaged in order to measure their performance specifications.

6.7 Summary

In this chapter, three g_m boosted source followers were developed, whose effective transconductance was boosted using current feedback. These source followers were able to achieve larger small-signal gain as well as bandwidth for lower power and device area. Through simulations and measurements, the performances of these source followers were verified.

The push-pull source follower was integrated with the un-buffered versions of *OP2* and *OP3* to convert them into buffered op amps so that they could drive large output capacitive loads. During fabrication, the process was updated, but the corresponding device models were not available during simulation. This had a major impact on the bias current generation circuits, which affected the overall operating points of the op amps as well as the output source followers. Even though the simulated performance of the buffered versions of *OP2* and *OP3* showed promising results, it could not be verified in the measurements due to improper biasing of various blocks of the buffered op amps. The overall performance of the un-buffered versions of the op amps were better than their buffered versions primarily because the output source follower stages of the op amps failed to operate satisfactorily due to updates in the fabrication process. With the prior knowledge of the updates in the fabrication process, further fabrication of the op amps is being carried out, but the results will not be included in this thesis.

Chapter 7

Contributions of the Research

The research in this thesis was aimed at investigating the feasibility of developing scalable analog circuit techniques across different technologies with small channel lengths. An op amp was chosen as an example circuit, and its small-signal gain, UGBW frequency and phase margin were chosen as the target performance specifications to be made constant across different technologies. It was also intended to perform the design with all small channel length devices. Based on this research, the various contributions are summarized below:

1. **Study of the feasibility of developing scalable op amps with all small channel length devices**

   The primary aim of the research was to develop scalable op amps, whose performance can be kept constant independent of technology as well as channel length of the devices. It was found that small channel lengths degrade overall circuit performance, and it is not recommended to use all small channel length devices. Moreover, while using minimum channel length devices, complete scalability of the op amps could not be achieved. If the performance specifications can be expressed as ratios (which can be made constant across different technologies), better scalability can be achieved by increasing the channel lengths from minimum feature size.

2. **Boost in the small-signal gain of a differential output stage using a negative resistance circuit**

Gain stages with small channel devices have poor gain, primarily caused by large channel length modulation effects associated with the MOS devices. A negative resistance circuit can be used to generate small-signal negative resistance based on the drain-to-source resistances of the MOS devices. This negative resistance can be used to cancel the positive drain-to-source resistances of the devices in the differential-in, differential-out gain stages and boost the overall output resistance of the gain stage. The extent of cancellation of the negative and positive resistances can be made controllable based on the bias currents.

3. **Constant unity-gain bandwidth and phase margin of the op amp**

When using a simple Miller compensation scheme, the unity-gain bandwidth of the op amp depends on the transconductance of the input devices and the compensation capacitor. The transconductance of the input NMOS devices of the differential input pair can be designed to depend on a resistor and ratio of device widths, which can be made independent of the technology. Further, the phase margin can be expressed as a ratio of NMOS transconductances, which can be kept constant across different technologies without changing any component in the circuit.

4. Current feedback, g_m boosted source followers

The output of the op amps can be buffered using source followers, whose effective transconductance can be boosted using current feedback. Comparing with the simple source followers, the current-feedback source followers can achieve larger gain as well as bandwidth for less input capacitance, overall area, and power. They are mainly suited for driving small loads (like, 50 Ω) with small-signal inputs, because they have poor distortion performance for large-signal inputs.

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